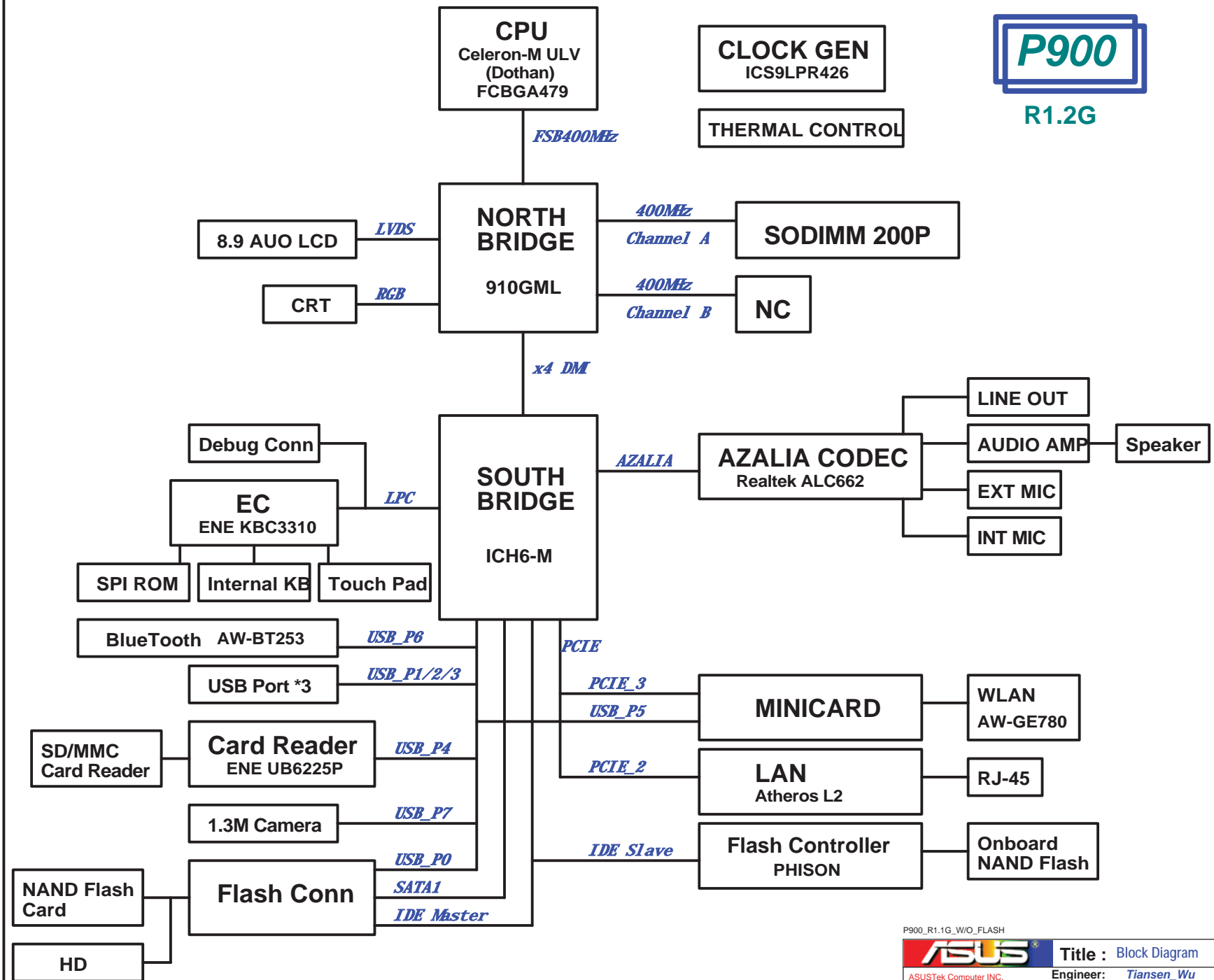


01\_Block Diagram  
02\_System Setting  
03\_Power Sequence  
04\_EC Pin Define  
05\_History  
06\_\*  
07\_Clock Gen\_ICS9LPR426  
08\_Dothan\_HOST  
09\_Dothan\_PWR\_GND  
10\_910GML\_HOST\_DMI  
11\_910GML\_DRAM  
12\_910GML\_VGA\_LVDS\_TV  
13\_910GML\_PWR  
14\_910GML\_GND  
15\_ICH6-M\_Azalia\_GPIO\_PCI\_LAN  
16\_ICH6-M\_USB\_PCIE\_DMI\_IDE\_SATA  
17\_ICH6-M\_PWR\_GND  
18\_DDR2 SODIMM  
19\_DDR2\_Termination  
20\_Onboard VGA  
21\_LCD Conn  
22\_Minicard  
23\_LAN\_Atheros L2  
24\_RJ45/BlueTooth  
25\_Onboard Flash  
26\_Flash Conn  
27\_USB Port  
28\_Card Reader\_ENE UB6225P  
29\_Camera Conn  
30\_Codec\_ALC662  
31\_Audio\_AMP\_Jack  
32\_EC\_ENE KB3310  
33\_Switch\_SPI ROM\_Debug Conn  
34\_KB\_Touch Pad  
35\_Thermal Sensor\_FAN  
36\_LED\_THERMTRIP  
37\_Discharge  
38\_PWR Jack  
39\_Srew Hole  
40\_EMI  
41\_POWER FLOW  
42\_CHARGER  
43\_VCORE(7A)  
44\_POWER\_3V\_5V\_VTT\_DDR  
45\_POWER\_3VA\_3VSB  
46\_POWER\_1.05V\_1.5V\_2.5V  
47\_POWER\_1.8V\_DUAL\_5VSB



P900\_R1.1G\_WO\_FLASH

		Title : Block Diagram	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008		Sheet	1 of 47

## ICH6 GPIO SETTING

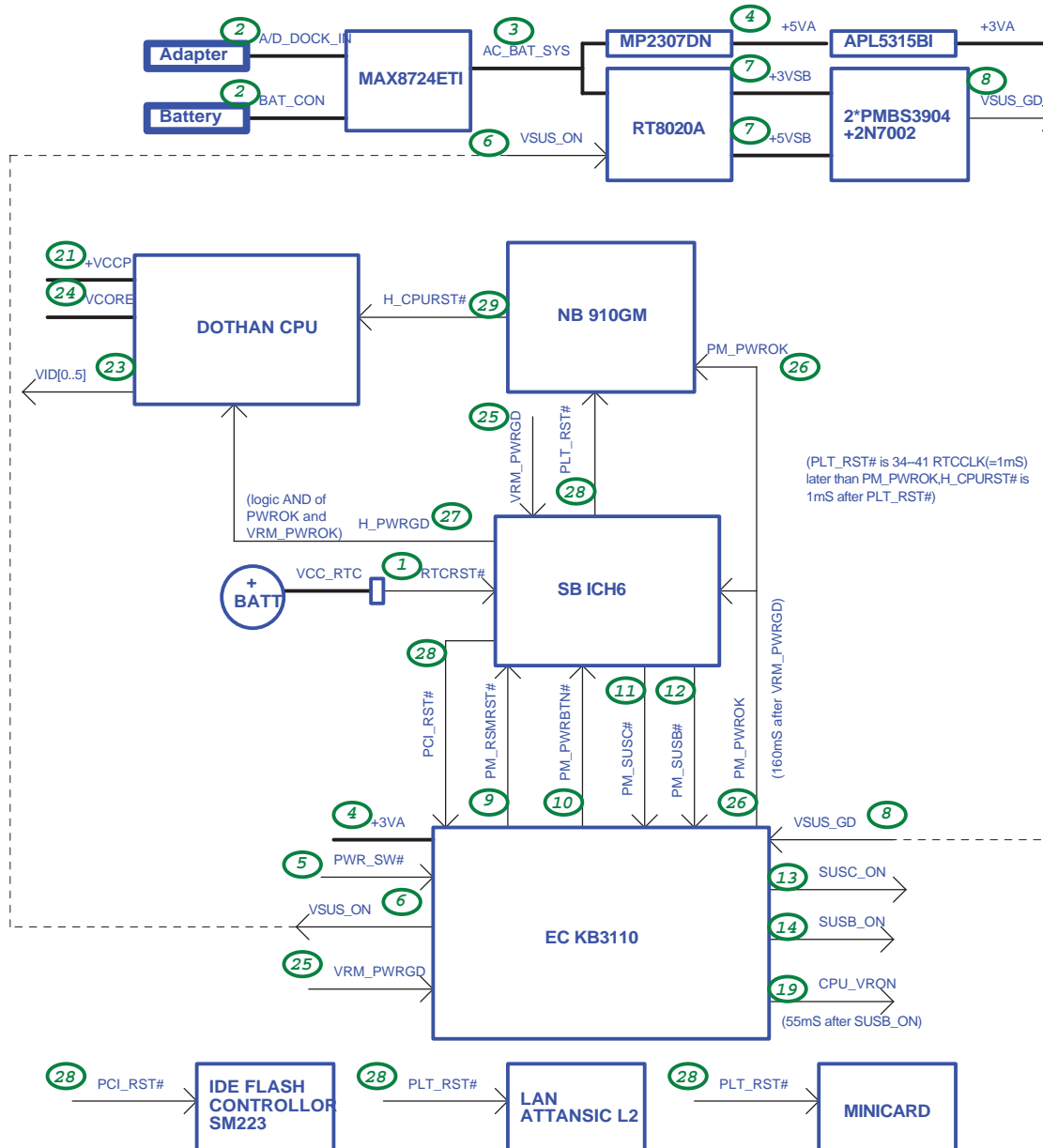
Pin	Pin Name	Connect to	Type	Input/Output Set
B7	GPIO/REQ6#	10K Pull +3V	I	fixed as Input only
E8	GP11 / REQ5#	10K Pull +3V	I	fixed as Input only
D9	GP12 / PIRQE#	10K Pull +3V	I	fixed as Input only
C7	GP13 / PIRQF#	10K Pull +3V	I	fixed as Input only
C6	GP14 / PIRQG#	10K Pull +3V	I	fixed as Input only
M3	GP15 / PIRQH#	10K Pull +3V	I	fixed as Input only
AD19	GP16 / BMBUSY#	NB BMBUSY#	I	Input
AE19	GP17	NC	GPI	fixed as Input only
R1	GP18	EC KBC_SCI#	GPI	fixed as Input only
C23	GP19/OC4#	10K Pull +3V	I	Input
D23	GP110/OC5#	10K Pull +3V	I	Input
W6	GP111 / SMBALERT#	S_SMBALERT#	I	Input
M2	GP112	NC	GPI	fixed as Input only
R6	GP113	EC EXTSMI#	GPI	fixed as Input only
C25	GP114/OC6#	10K Pull +3V	I	Input
C24	GP115/OC7#	10K Pull +3V	I	Input
D8	GPO16/GTN6#	NC	O	Output
F6	GPO17 / GNT5#	NC	O	Output
AC21	GPO18 / STP_PC#	Clock GEN STP_PC#	O	Output
AB21	GPO19	WLAN_LED#	GPO	fixed as Output only
AD22	GPO20 / STP_CPU#	STP_CPU#	O	Output
AD20	GPO21	CAMERA_EN	GPO	fixed as Output only
NA	GPIO22	NC	NA	NA
AD21	GPO23	SPEAKER_EN#	GPO	fixed as Output only
V3	GPIO24	MINICARD_EN#	I/O	Output
P5	GPIO25	WLAN_ON#	I/O	Output

Pin	Pin Name	Connect to	Type	Input/Output Set
AF17	GP126/SATA0GP	NC	GPI	(GPI)Input
R3	GPIO27	CARD_READER_EN#	I/O	Output
T3	GPIO28	NC	I/O	Output
AE18	GP129 / SATA1GP	PCBVER0	GPI	(GPI)Input
AF18	GP130 / SATA2GP	NC	GPI	(GPI)Input
AG18	GP131 / SATA3GP	PCBVER1	GPI	(GPI)Input
AF19	GPIO32 / CLKRUN#	10K Pull +3V	I/O	Input
AF20	GPIO33	PM_VCOREL1	I/O	Output
AC18	GPIO34	PM_VCOREL2	I/O	Output
NA	GPIO35	NA	NA	NA
NA	GPIO36	NA	NA	NA
NA	GPIO37	NA	NA	NA
NA	GPIO38	NA	NA	NA
NA	GPIO39	NA	NA	NA
F7	GP140 / REQ4#	10K Pull +3V	I	Input
P4	GP141 / LDRQ1#	NC	I	Input
NA	GPIO42	NA	NA	NA
NA	GPIO43	NA	NA	NA
NA	GPIO44	NA	NA	NA
NA	GPIO45	NA	NA	NA
NA	GPIO46	NA	NA	NA
NA	GPIO47	NA	NA	NA
E7	GPO48 / GNT4#	NC	O	Output
AC25	GPO49 / CPUPWRGD	CPU Power Ok	O	Output

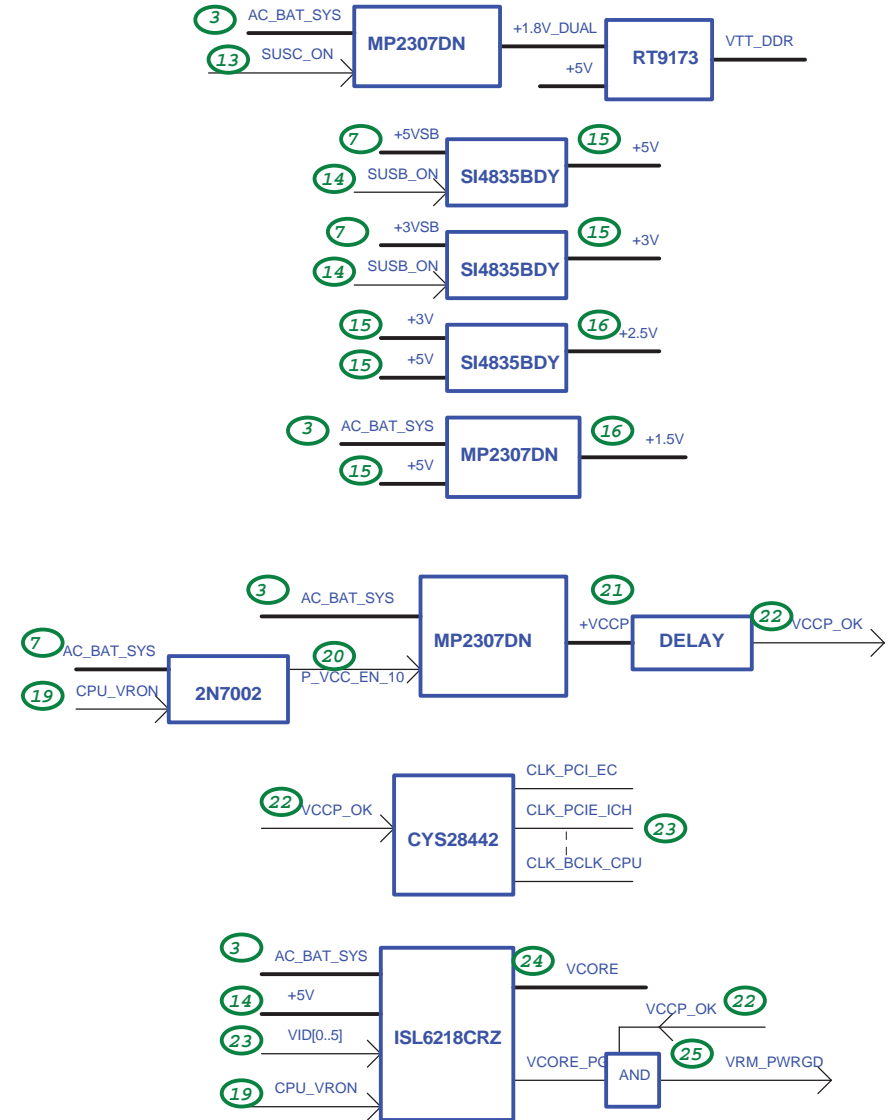
P900\_R1.1G\_W/O\_FLASH

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name		Rev
A3	P900		1.2G
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\*This sequence is for Battery Plug-in and no Adapter,  
if Adapter Plug-in, the sequence change to:  
A/D\_DOCK\_IN-->AC\_BAT\_SYS-->+3VA-->VSUS\_ON-->+3VSB & +5VSB  
-->VSUS\_GD-->PM\_REMRST#-->PWR\_SW#-->PM\_PWRBTN-->PM\_SUSC#-->PM\_SUSB#



	Signal	S0/S1	S3	S4/S5	Power
Only Battery	VSUS_ON	H	H	L	VSUS
Adapter In	VSUS_ON	H	H	H	VSUS
	SUSB_ON	H	L	L	Main
	SUSC_ON	H	H	L	DUAL



P900\_R1.1G\_WO\_FLASH

<b>ASUS</b>		Title : Power Sequence	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
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## EC KB3310 GPIO SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
1	GA20	A20GATE	O	A20GATE
2	KBRST#	RC_IN#	O	KBRST#
6	GPIO04	EMAIL_SW#	I	EMAIL_SW#, *
13	PCIRST#	PCI_RST#	I	PCI Reset
14	GPIO07	BAT_EXT	O	Reserved
15	GPIO08	EXTSMH#	O	EXTSMH#, 10K Pull +3VSUS
16	GPIO0A	LID_EC#	I	LID_EC#, *
17	GPIO0B	NC	O	LCD chip select
18	GPIO0C	NC	I/O	LCD Data
19	GPIO0D	DISTP_SW#	I	Touch Pad Disabled, *
20	SC#	KBC_SC#	O	KBC_SC#, 10K Pull +3VSUS
21	PWM1	BL_PWM_DA	O	LCD Light Switch
23	PWM2	BAT_CRITICAL	O	LCD clock
25	GPIO11	PM_PWRBTN#	OD	Power Button to SB, *
26	FANPWM1	FAN0_PWM	O	CPU Fan(Unused)
27	FANPWM2	FAN1_PWM	O	VGA Fan(Unused)
28	FANFB1	FAN0_TACH	I	CPU FanTach(Unused)
29	FANFB2	FAN1_TACH	I	VGA FanTach(Unused)
30	GPIO16	E51_TX	O	RS232 debug port
31	GPIO17	E51_RX	O	Reserved
32	GPIO18	PWR_SW#	I	power button, *
34	GPIO19	MAIL_LED#	O	Mail LED(Unused)
36	GPIO1A	NUM_LED#	O	EC H/W controls(Unused)
38	CLKRUN#	N.C	O	Reserved
39	KSO0	KSO0	O	For Keyboard interface
40	KSO1	KSO1	O	For Keyboard interface
41	KSO2	KSO2	O	For Keyboard interface
42	KSO3	KSO3	O	For Keyboard interface
43	KSO4	KSO4	O	For Keyboard interface
44	KSO5	KSO5	O	For Keyboard interface
45	KSO6	KSO6	O	For Keyboard interface
46	KSO7	KSO7	O	For Keyboard interface
47	KSO8	KSO8	O	For Keyboard interface
48	KSO9	KSO9	O	For Keyboard interface
49	KSO10	KSO10	O	For Keyboard interface
50	KSO11	KSO11	O	For Keyboard interface
51	KSO12	KSO12	O	For Keyboard interface
52	KSO13	KSO13	O	For Keyboard interface
53	KSO14	KSO14	O	For Keyboard interface
54	KSO15	KSO15	O	For Keyboard interface
55	KSI0	KSI0	I	For Keyboard interface
56	KSI1	KSI1	I	For Keyboard interface
57	KSI2	KSI2	I	For Keyboard interface
58	KSI3	KSI3	I	For Keyboard interface
59	KSI4	KSI4	I	For Keyboard interface
60	KSI5	KSI5	I	For Keyboard interface
61	KSI6	KSI6	I	For Keyboard interface
62	KSI7	KSI7	I	For Keyboard interface
63	AD0	BAT_ICHG	I	Sense Power Loading
64	AD1	BAT_CONFIG	I	sense Battery
65	AD2	BAT_SENT	I	Reserved
66	AD3	BAT_TS	I	Reserved
68	GPO3C	DOC	O	Trigger Clock Gen

Pin No.	Pin Name	Signal Name	Type	NOTE
70	GPO3D	LCD_BACKOFF#	O	LCD_BACKOFF#
71	GPO3E	CLK_PWRSERVE#	O	Active when BAT_IN=1 and AC_OK=0(Unused)
72	GPO3F	PM_BATLOW#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K Pull GND
75	GPIO42	N.C	O	Reserved
76	GPIO43	N.C	O	Reserved
77	SCL1	SMB1_CLK	I/OD	4.7K Pull +3VA_EC
78	SDA1	SMB1_DAT	I/OD	4.7K Pull +3VA_EC
79	SCL2	SMB2_CLK	I/OD	10K Pull +3VS
80	SDA2	SMB2_DAT	I/OD	10K Pull +3VS
81	KSO16	N.C	O	Reserved
82	KSO17	N.C	O	Reserved
83	PSCLK1	LCD_SCL	O	Reserved
84	PSDAT1	LCD_SDA	O	Reserved
85	PSCLK2	LCD_CSB	O	Reserved
86	PSDAT2	LCD_VSYNC	O	Reserved
87	PSCLK3	TP_CLK	I/OD	10K Pull +3VS
88	PSDAT3	TP_DAT	I/OD	10K Pull +3VS
89	GPIO50	BATSEL_3S	O	Battery series, Hi:3S, Lo:4S(Unused)
90	GPIO52	CHG_LED_UP#	O	charger LED
91	GPIO53	CAP_LED#	O	EC H/W controls
92	GPIO54	PWR_LED_UP	O	EC H/W blinking
93	GPIO55	SCRL_LED#	O	EC H/W controls
95	GPIO56	PWR4G_SW#	I	*
97	GPXOA00	SPI_MODE#	O	*HW Strap for SPI Flash deExternal Pull Down 100K ohm to GND"
98	GPXOA01	SUSC_ON	O	
99	GPXOA02	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	PWROK	O	
103	GPXOA06	PM_LEVELDOWN#	O	Reserved
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0	BATSEL_2P#	O	Battery parallel, Hi:1P, Lo:2P-3P
110	GPXID1	CPU_LEVELDOWN#	O	Reserved
112	GPXID2	THRO_CPU	O	Active if Battery Temperature is over spec
114	GPXID3	SUSB#	I	Pull Down 100K ohm to GND
115	GPXID4	SUSC#	I	Pull Down 100K ohm to GND
116	GPXID5	CPUPWR_GD	I	10K Pull +3VS
117	GPXID6	VSUS_GD	I	Disabled **
118	GPXID7	BAT_VOLSEL	O	Reserved
121	GPIO57	INTERNET#	I	*
126	SPICLK	SPI_CLK	O	SPI Clock
127	GPIO59	N.C	O	Reserved

## EC KB3310 Other Pin SETTING

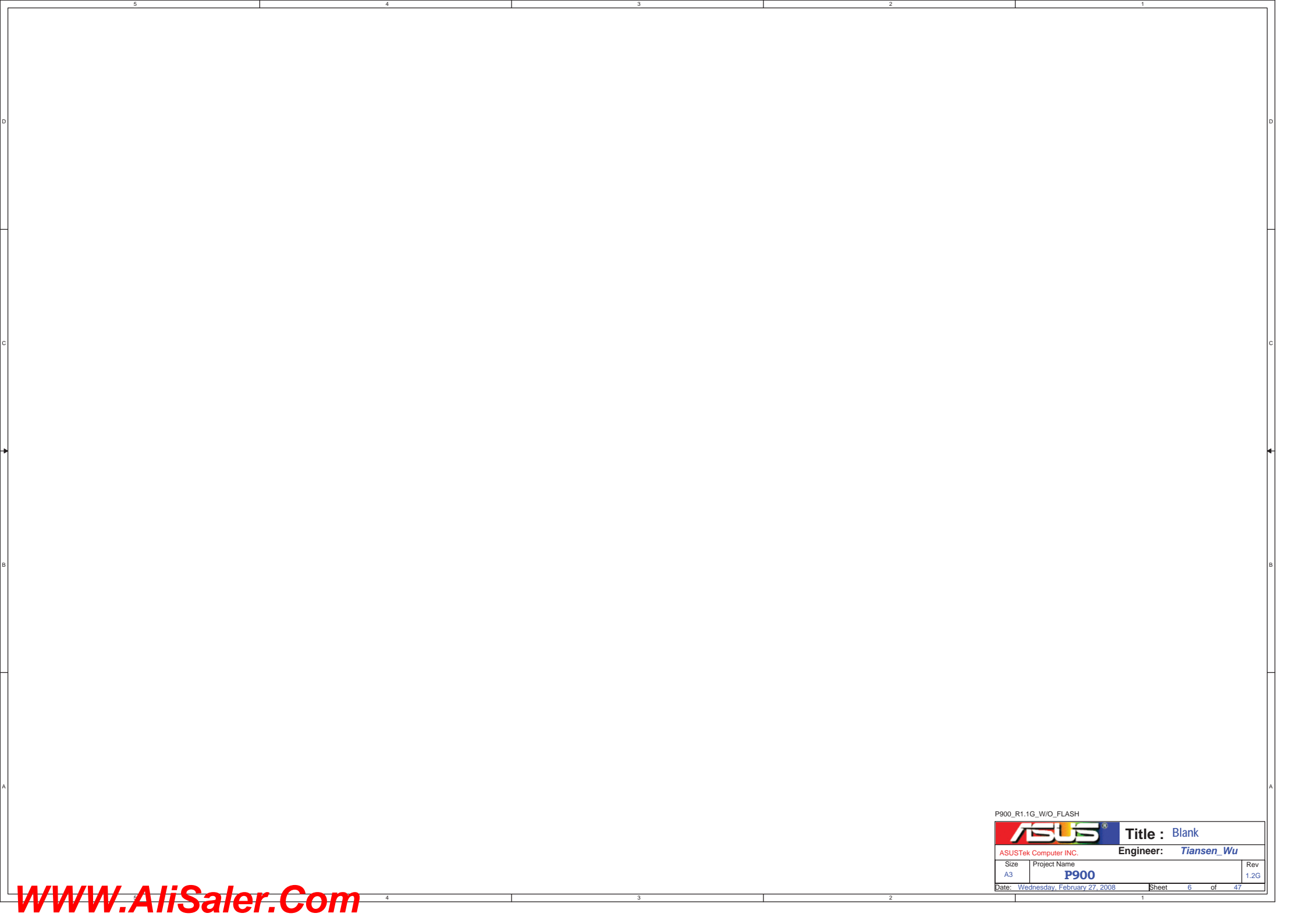
Pin No.	Pin Name	Signal Name	Type	NOTE
3	SERIRQ	INT_SERIRQ	I/OD	8.2K Pull +3VS
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	Add 100K ohm to GND
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#	SPI_SO	I	
120	WR#	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	K_V18R		Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#	SPI_CE#	O	


P900\_R1.1G\_W/O\_FLASH

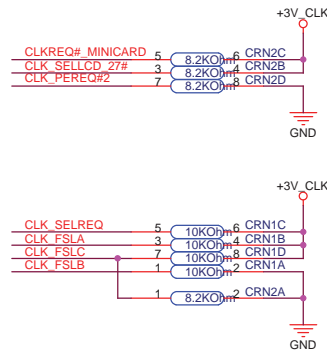
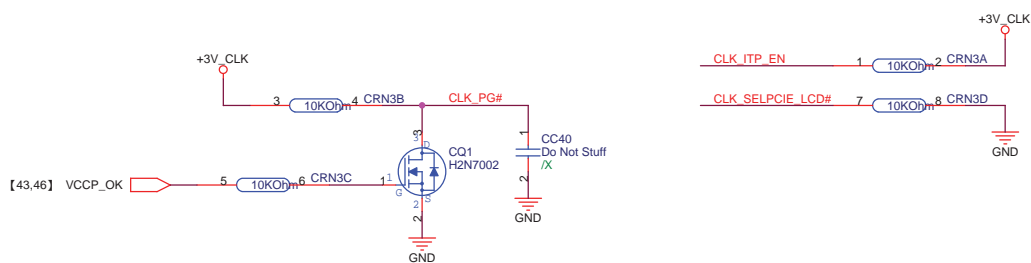
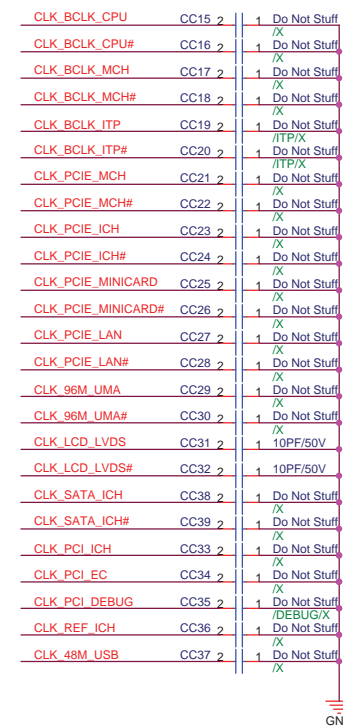
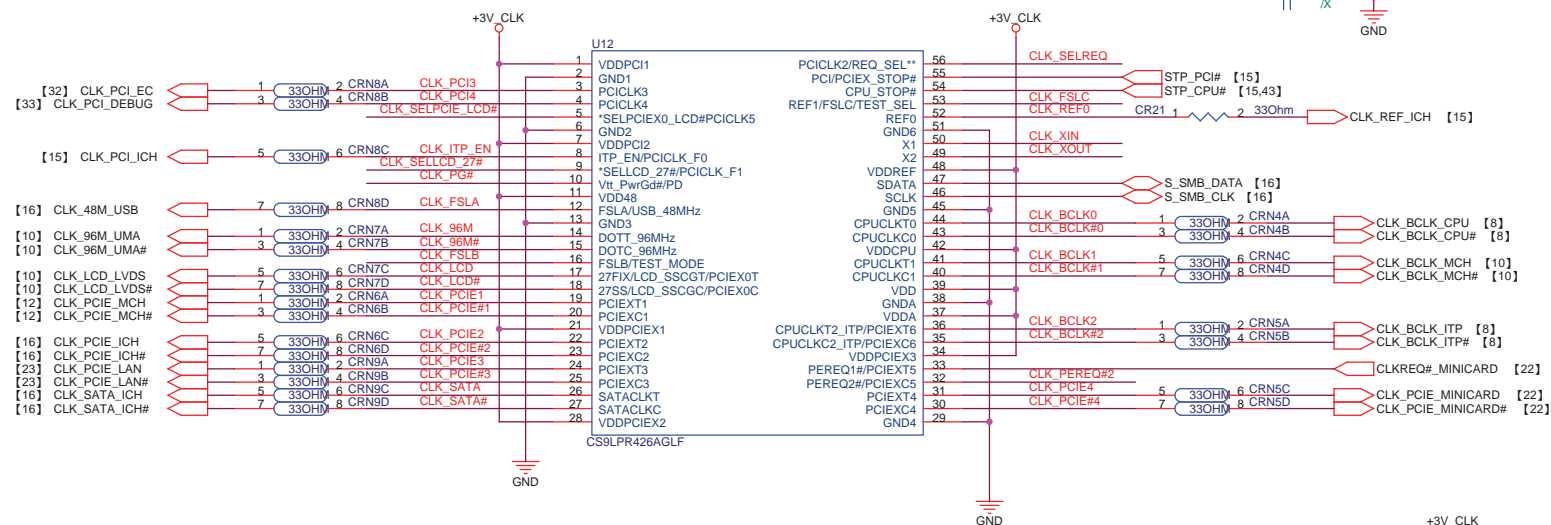
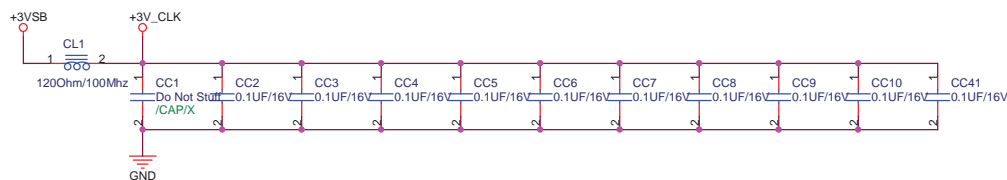
<b>ASUS</b>		Title : EC Pin Define		
ASUSTek Computer INC.		Engineer: Tiansen_Wu		
Size	Project Name		Rev	
A3	P900		1.2G	
Date: Wednesday, February 27, 2008		Sheet	4	of 47

Rev	Date	Description
<b>1.0G</b>	2007/02/26 }	S701L Schematic 1.0G Beginning
	2007/03/16	S701L 1.0G Gerber Out
<b>1.1G</b>	2007/03/24 }	S701L Schematic 1.1G Beginning
	2007/04/19	S701L 1.1G Gerber Out
<b>1.0G</b>	2007/04/24 }	<p>P701(S701L renamed) Schematic 1.0G Beginning</p> <ol style="list-style-type: none"> <li>1. PC8054, PR6075 /X to N/A</li> <li>2. Attansic L2 change to Atheros L2(pin to pin)</li> <li>3. LC1, LC33 /CAP/X to N/A</li> <li>4. C87 change to X5R to cost down</li> <li>5. L1, L2, L3 change to 56 NH, R5, R6 change to 75 Ohm to pass CRT EA measure</li> <li>6. PR48 change to 22K Ohm, PC35 change to 4700PF to fix no VCORE issue</li> <li>7. PR6074 change to 4.7K Ohm to fix +3VSB OCP issue</li> <li>8. Clock Gen CY28442-2 change to ICS9LPR367</li> <li>9. Phase in Power Level Reduce solution, mark "Taipei0508"</li> <li>10. Card Reader Socket change to SD Socket 12G25100091E</li> <li>11. Add System FAN circuit</li> <li>12. Camera change to USB port 7, Minicard change to USB port 5</li> <li>13. Use SB GPIO27 to Enable/Disable Card Reader UB6225P</li> <li>14. Use SB GPIO28 to Enable/Disable Modem</li> <li>15. Card Reader UB6225P share 48M clock from CLock Gen with SB USB part</li> <li>16. Add D29 to fix LCD_CSB leakage current issue</li> <li>17. LC29, LC30 change to 27PF to pass EA crystal measure</li> <li>18. Change vaule of PR73, PR74, PC56 and add PC60 to adjust the power sequence timing</li> <li>19. Remove USB port 1</li> <li>20. Add +5V generate +3V_LCD circuit</li> <li>21. Remove +5V_CHG generate circuit</li> <li>22. Use SB GPIO33, GPIO34 to controll the level of VCORE</li> <li>23. U31 use APL5315BI-TRL to replace MAX8863TEUK(pin to pin, but reference voltage level different)</li> <li>24. PR59 change to 130K Ohm for both 12V Adapter and 9.8V Adapter</li> </ol>
	2007/05/22	P701 1.0G Gerber Out
<b>1.1G</b>	2007/05/31 }	<p>P701 Schematic 1.1G Beginning</p> <ol style="list-style-type: none"> <li>1. Remove the 48M clock from CLock Gen to Card Reader UB6225P</li> <li>2. Clock Gen ICS9LPR367 change to ICS9LPR426</li> <li>3. Flash Connector increase SATA and USB interface</li> <li>4. Add Onboard Flash(SM223 + NAND Flash x4)</li> <li>5. BATT_CON pin 5 connect to GND</li> <li>6. Q34 pin 1 connect to +3V to fix EC reset issue</li> <li>7. Remove J1, J2</li> <li>8. KB pin 28 connect to GND for P701-ISP_CARD</li> <li>9. Use SB GPO23 to Enable/Disable Audio Amplifier</li> <li>10. Use SB GPO21 to controll Camera Power</li> <li>11. Use SB GPIO24 to controll Minicard Power</li> <li>12. Use SB GPIO25 to Enable/Disable WLAN Ratio</li> <li>13. Atheros L2 and Minicard SMBUS interface directly pull high</li> <li>14. LCD_CON pin 20 connect to AC_BAT_SYS</li> </ol>
	2007/06/07	P701 1.1G Gerber Out

Rev	Date	Description
1.2G	2007/06/30 { }	<p>P701 Schematic 1.2G Beginning</p> <ol style="list-style-type: none"> <li>1. Add R174 to short DASP pins of Master IDE device and SLave IDE device</li> <li>2. Use SB GPIO27 to controll Card Reader UB6225P Power</li> <li>3. PR606084.2 connect to +5V to fix LCD flash issue</li> <li>4. Adjust SPEAKER pin define</li> <li>5. Adjust CHARGE LED and WLAN LED lightness</li> <li>6. Use SB GPI 26, 29, 30, 31 for PCB version</li> <li>7. Change USB ESD diode for EMI request</li> <li>8. Add Floating GND TP_GND and Spring TP1 &amp; TP2 for EMI request</li> <li>9. Change PM_VCOREL1, PM_VCOREL2 default level</li> <li>10. Add PQ48 to controll +3V_PE to fix WLAN AW-GE780 can't detect issue</li> <li>11. Power Charger part update circuit for new Adapter</li> <li>12. Use SB GPI12 to detect LID signal level</li> <li>13. Add H/W THERMTRIP circuit (page 36)</li> <li>14. Add U40 to prevent system auto power on after clear CMOS</li> <li>15. Use SB GPI7 for THRO_CPU</li> <li>16. Power Charger part update circuit to prevent incorrect Adapter damage boards</li> <li>17. Q1.1, Q2.1 change to +3V</li> </ol> <p>P701 1.2G Gerber Out</p>
1.2G	2007/07/26 { }	<p>P701 Schematic 1.3G Beginning</p> <ol style="list-style-type: none"> <li>1. Add R11 for 801</li> </ol>

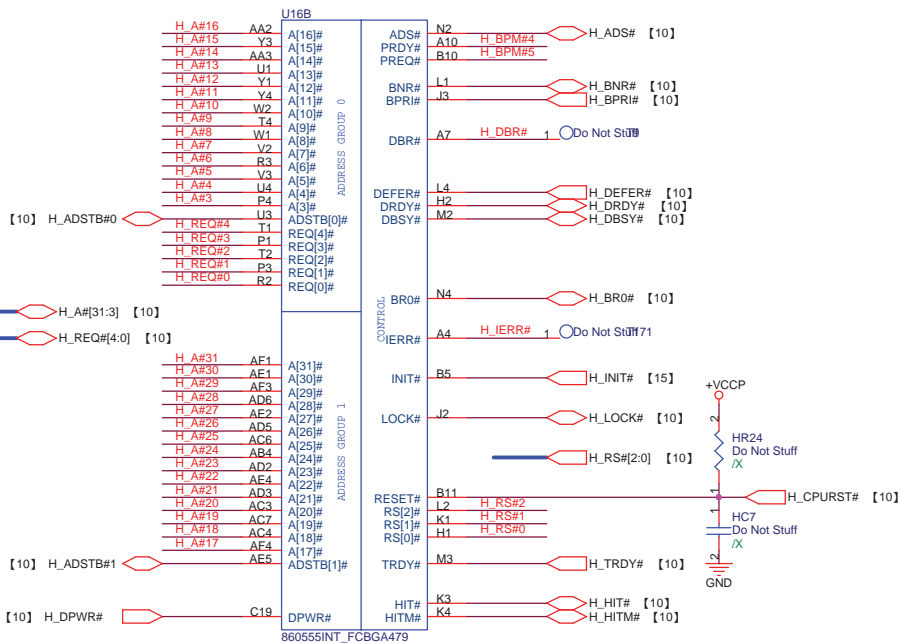


P900_R1.1G_W/O_FLASH			
		Title : Blank	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008		Sheet	6 of 47

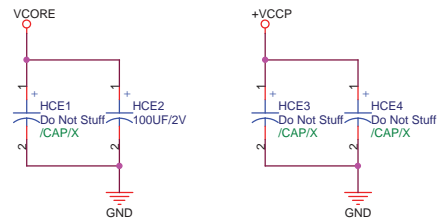
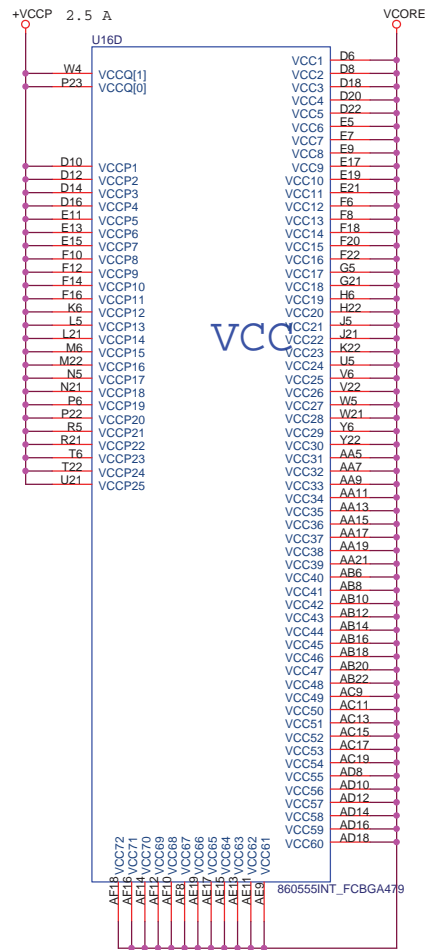


	100MHz	133MHz
FSLA	1	1
FSLB	0	0
FSLC	1	0

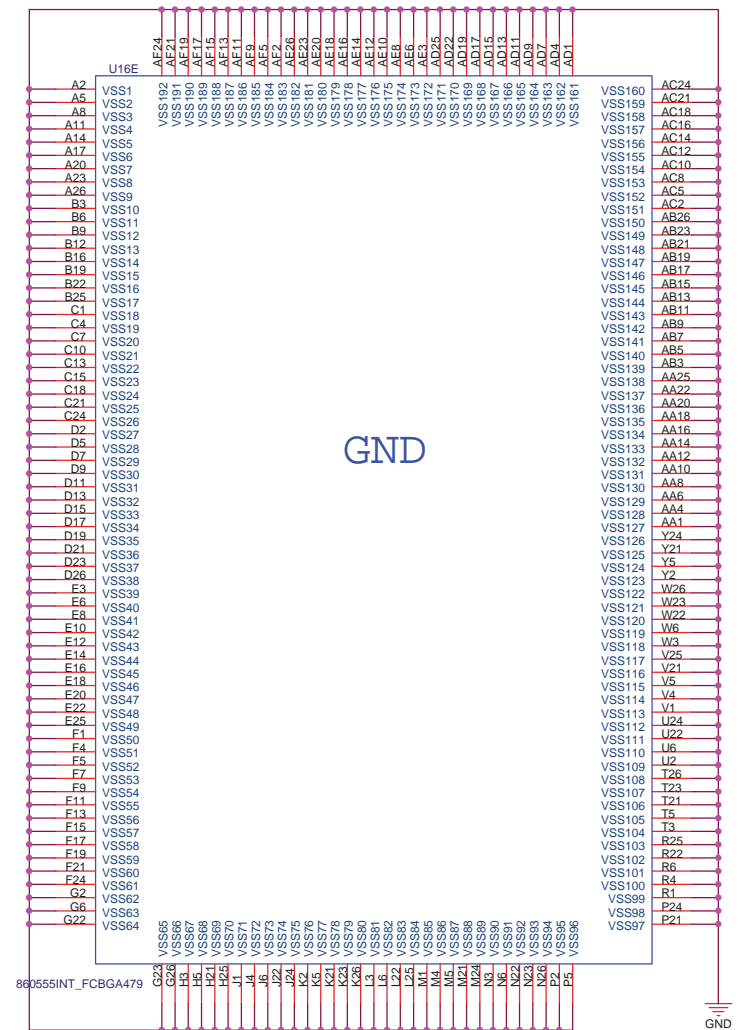
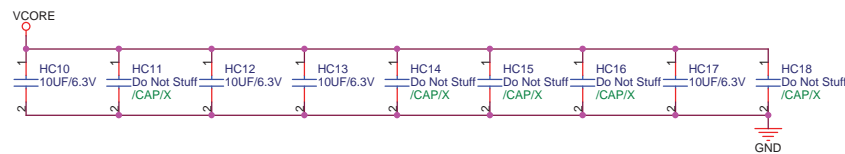
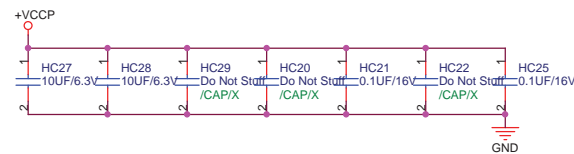
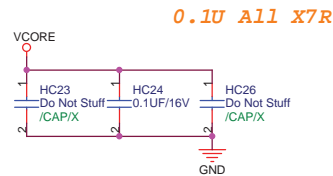




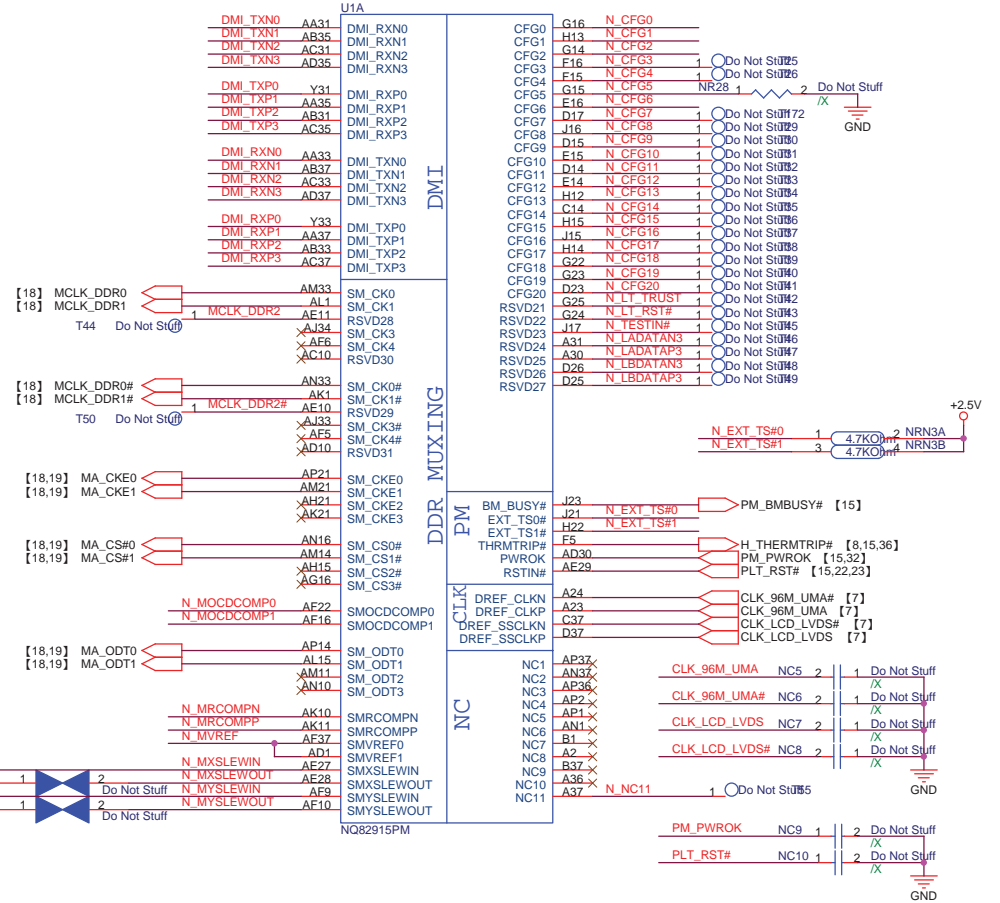
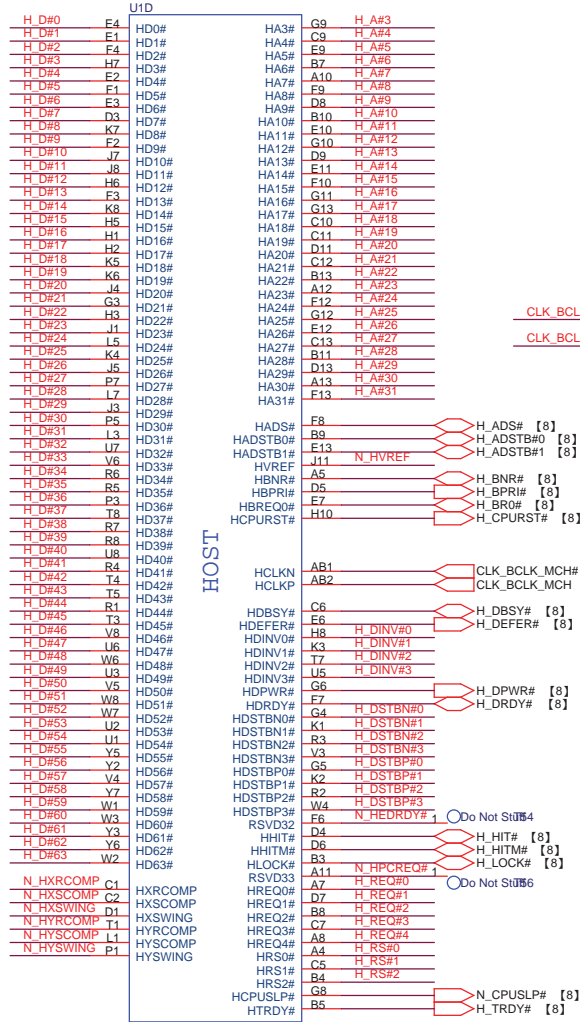
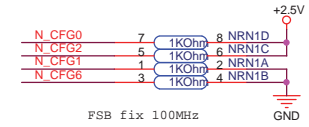
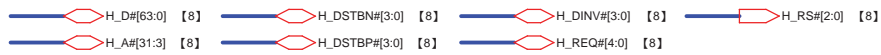




U16 use 01G011920000PM

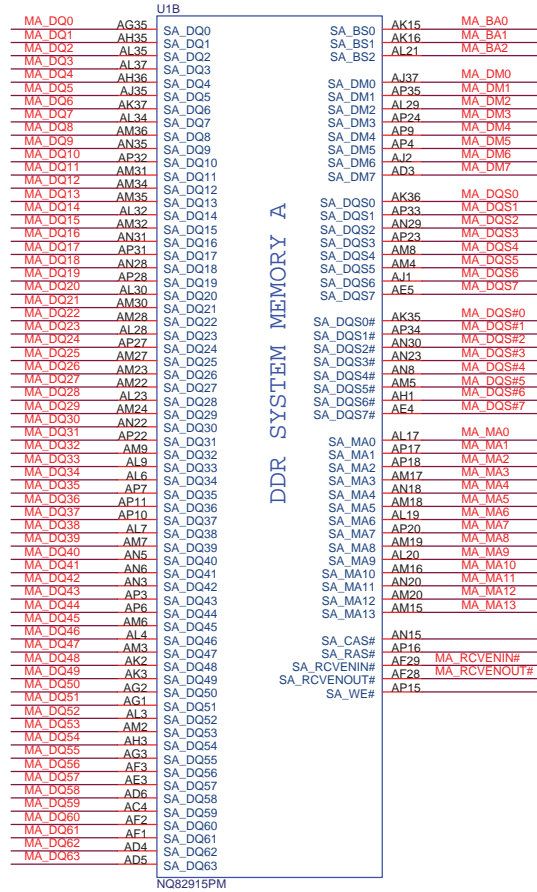


P900\_R1.1G\_WO\_FLASH

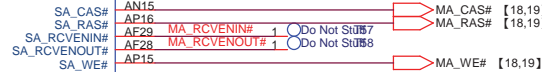




U1 use 02G010007612



DDR SYSTEM MEMORY A



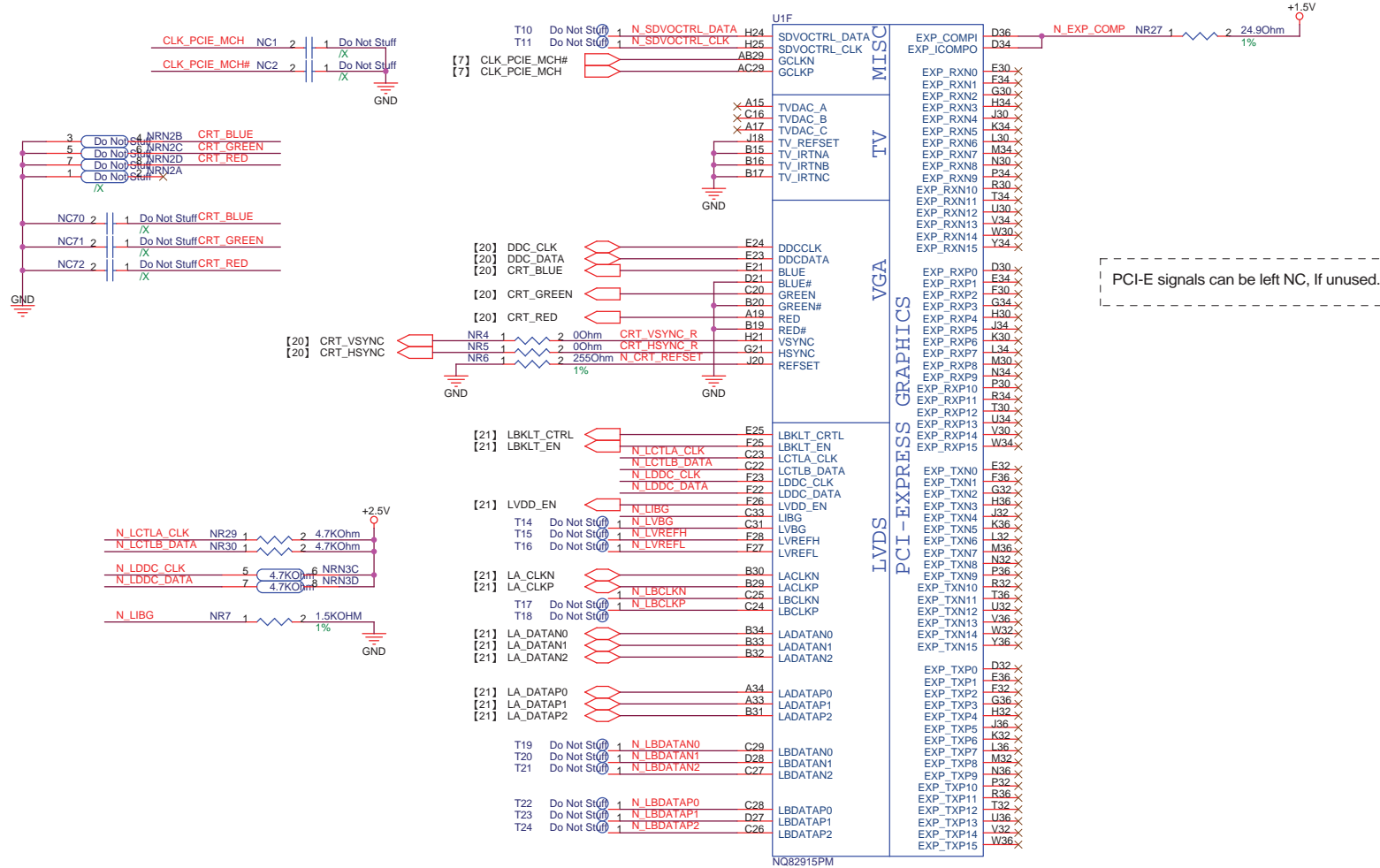
DDR SYSTEM MEMORY B

P900\_R1.1G\_W/O\_FLASH

SDVO Smbus have  
internal pull down

SDVOCTRL\_DATA Int PD  
0 : No SDVO device  
1 : SDVO device present

U1 use 02G010007612



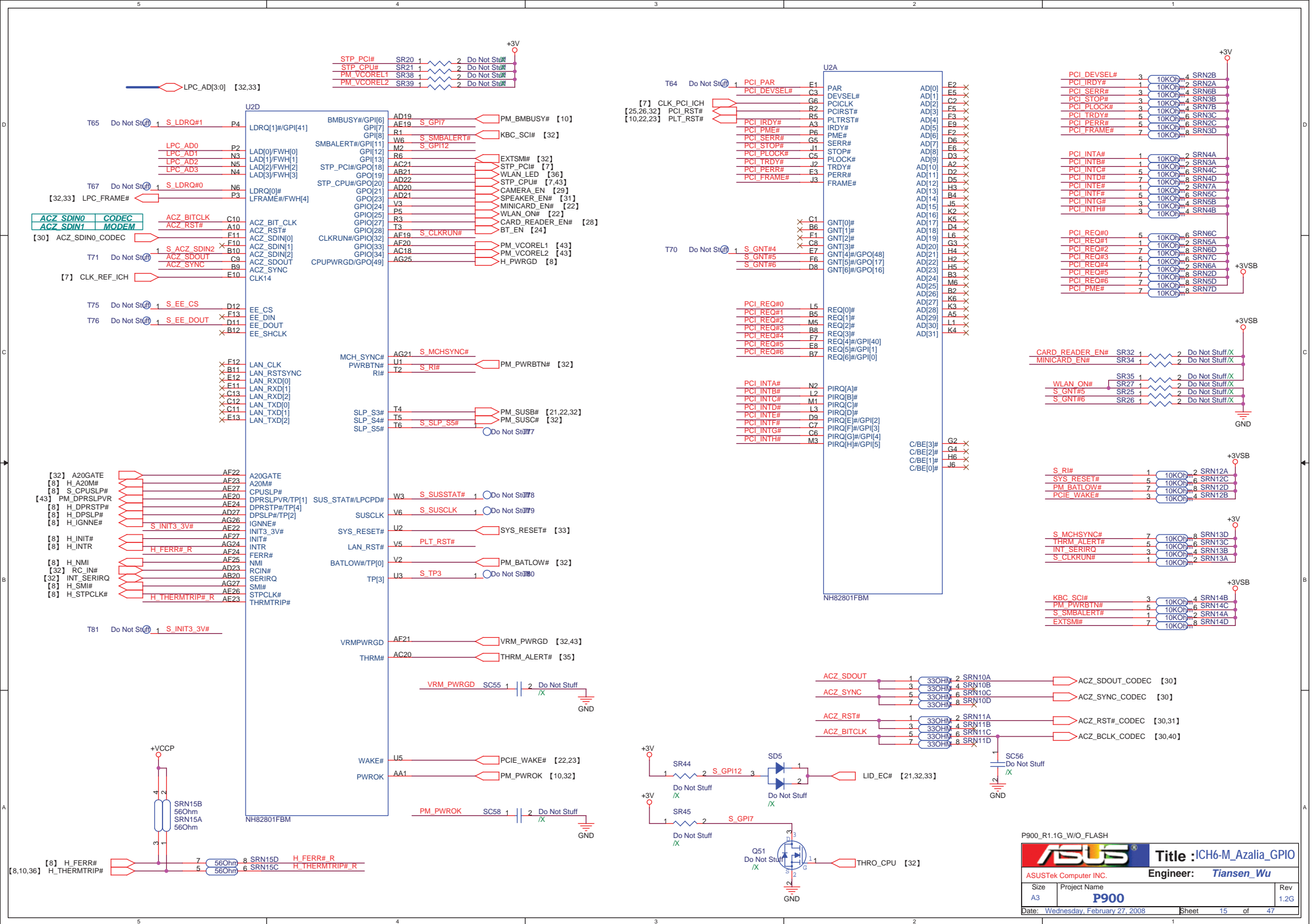
P900\_R1.1G\_WO\_FLASH

ASUS®		Title : 910GML_VGA_LVDS	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	12 of 47



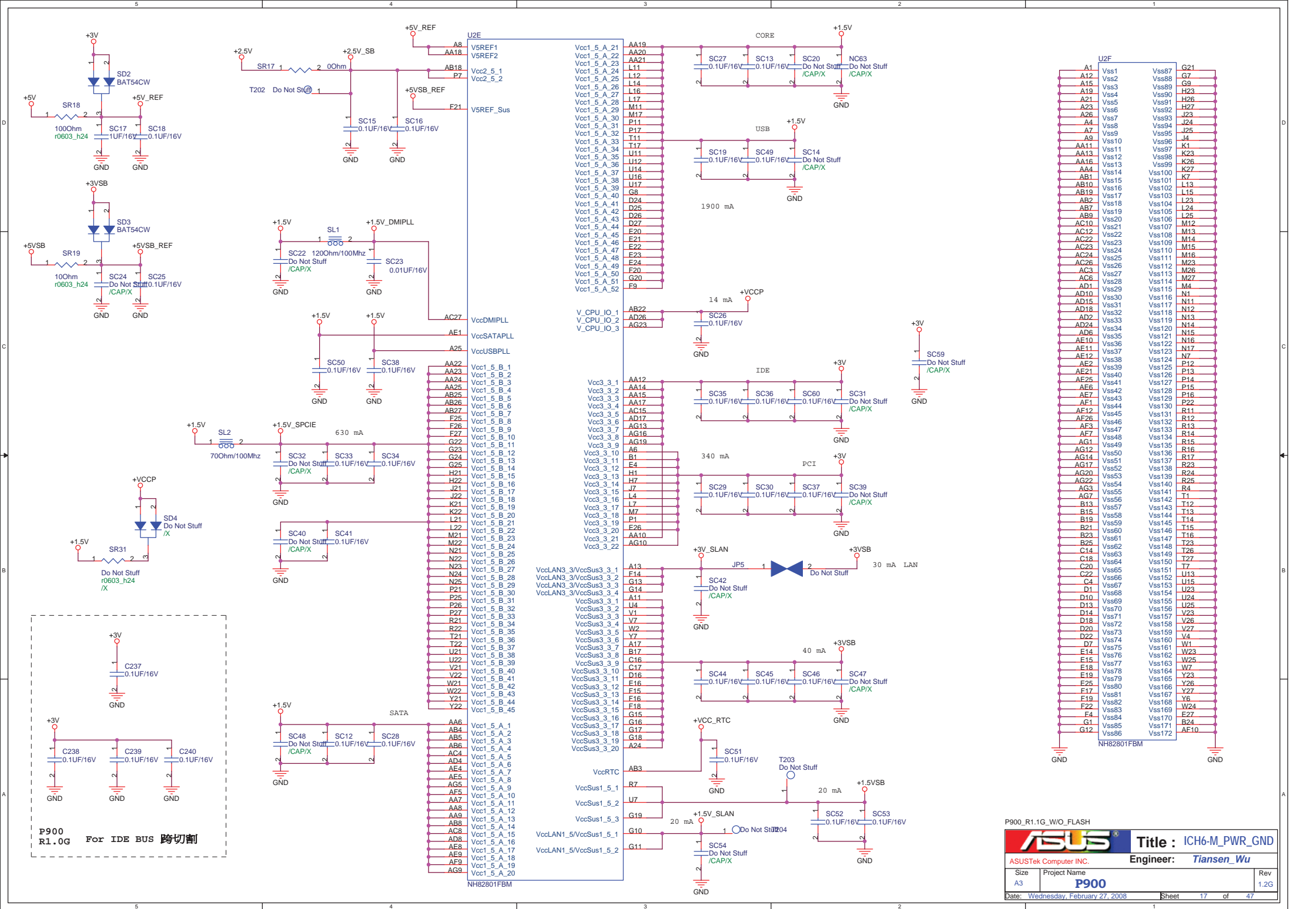


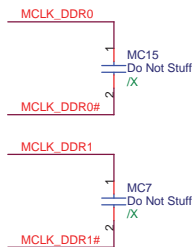




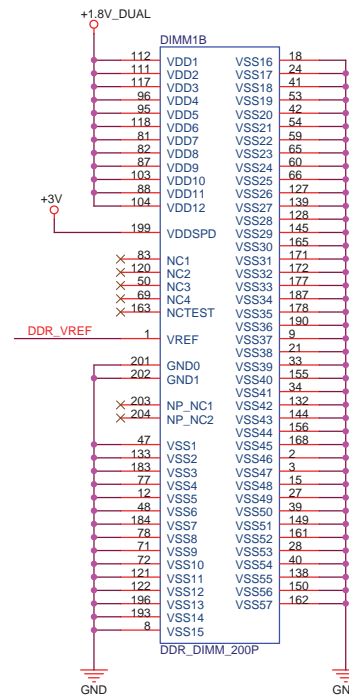
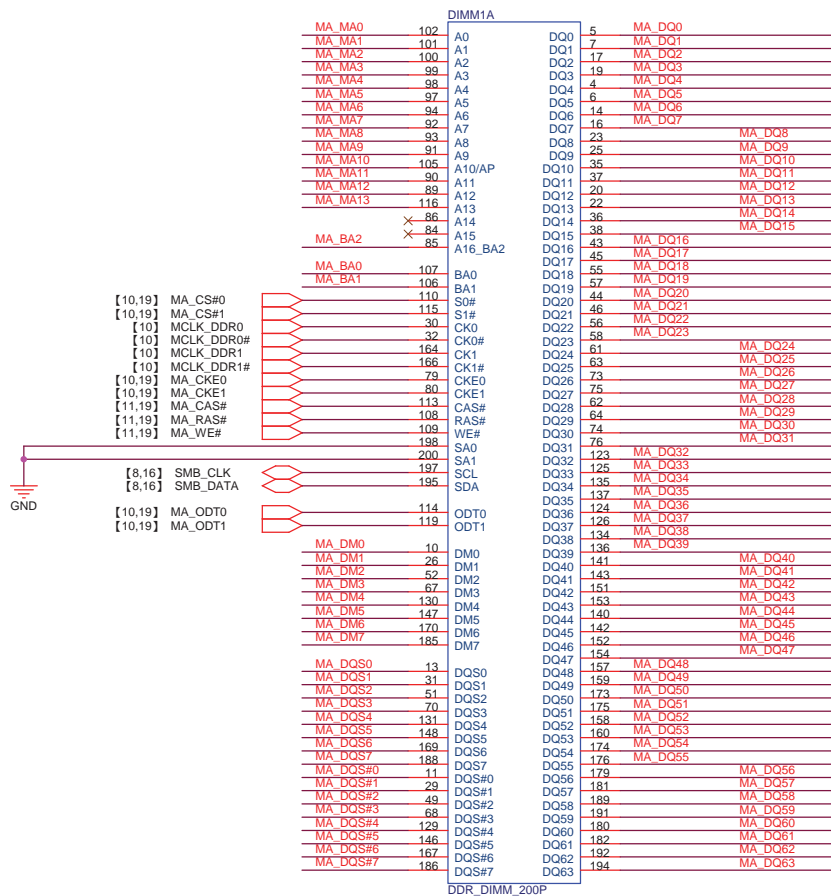
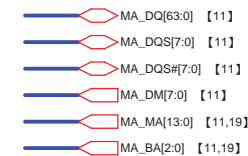


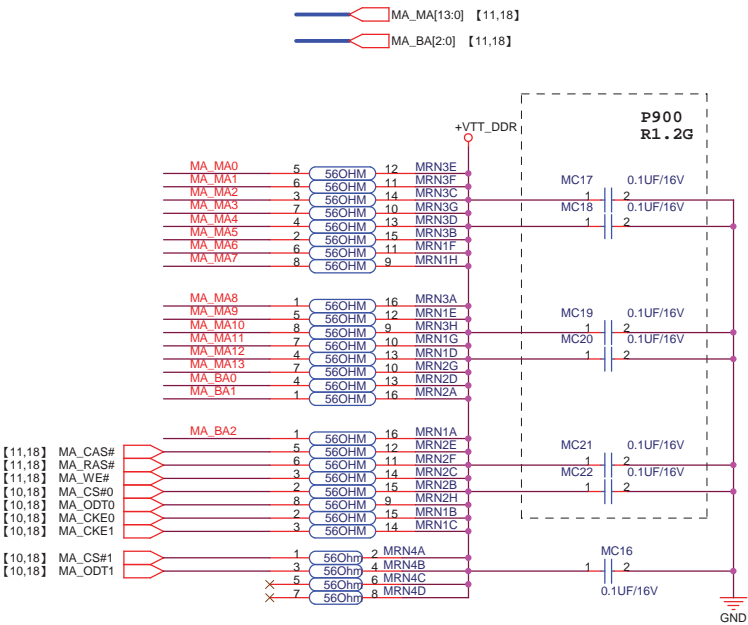






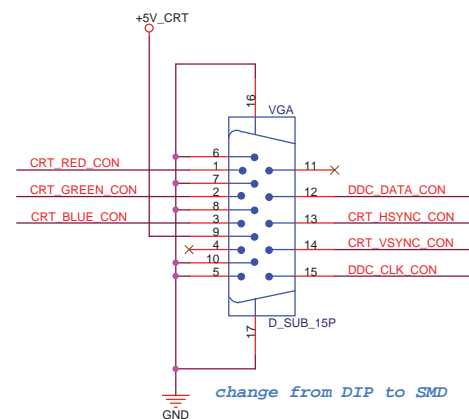
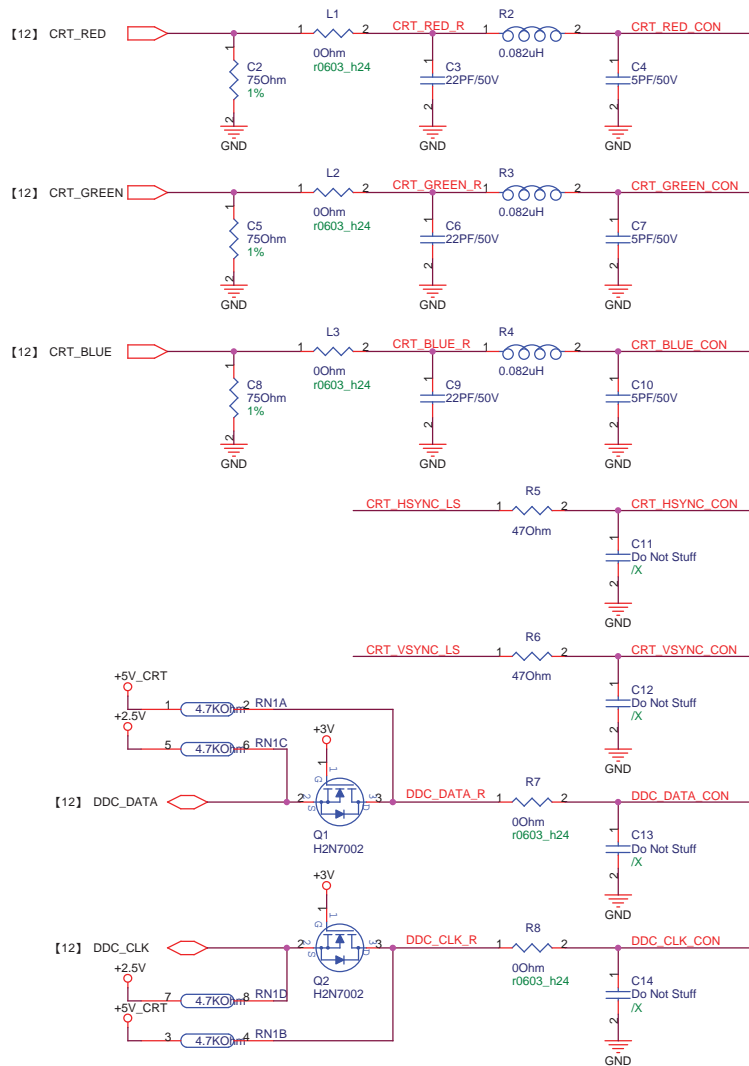
STD Type



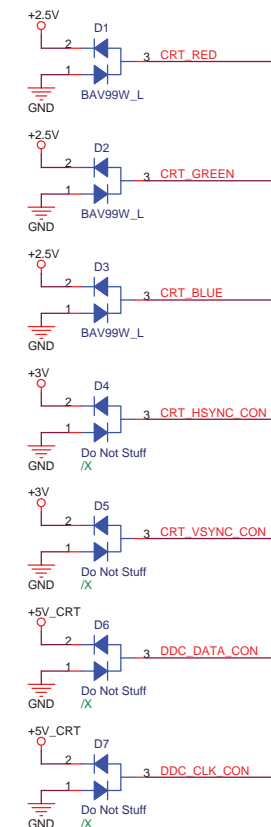
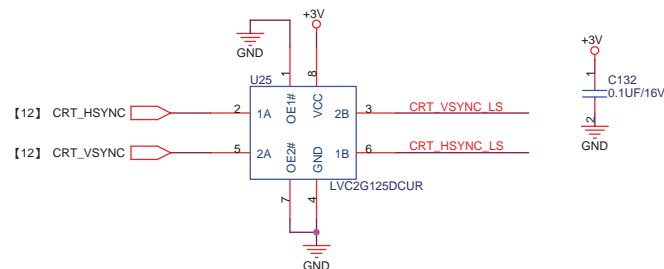


P900\_R1.1G\_WO\_FLASH

<b>ASUS</b>		Title : DDR2_Termination	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008		Sheet	19 of 47

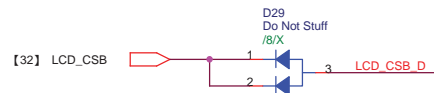


VGA use 12G10110015W & 12G10110015N

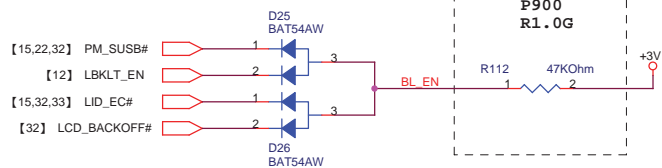
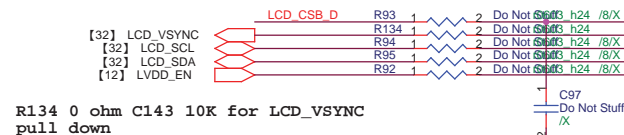


P900\_R1.1G\_WO\_FLASH

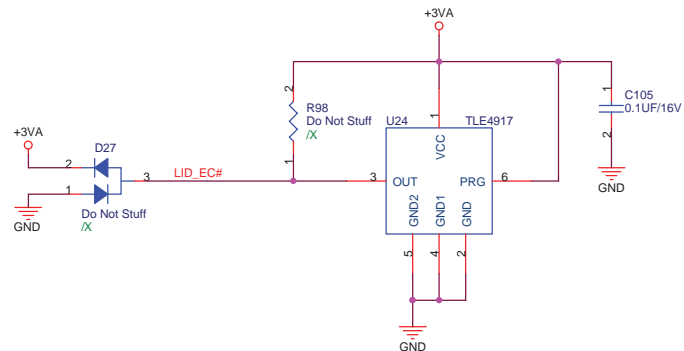
ASUS		Title : Onboard VGA	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	20 of 47



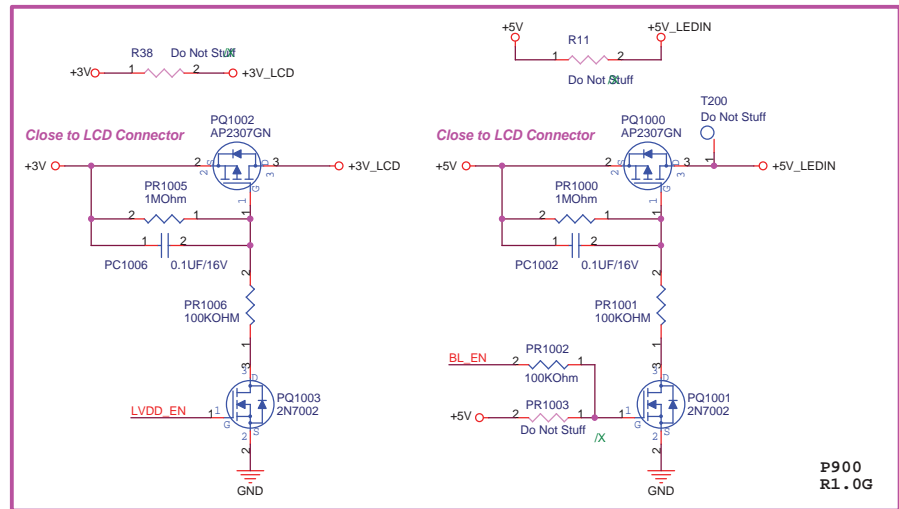
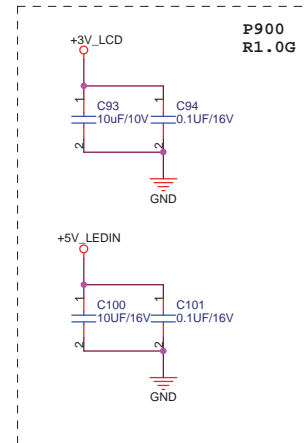
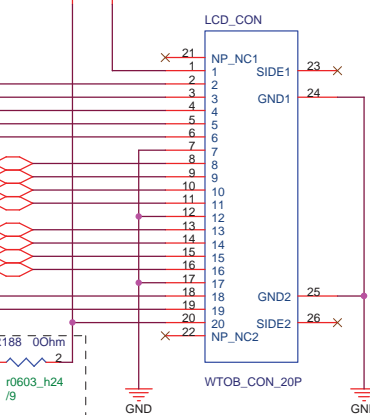
Remove R134 for LCD Board 1.4G, need rework



### Hall Switch

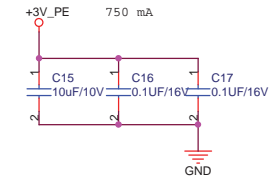


LCD\_CON use 12G171040204

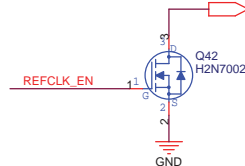
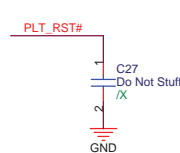
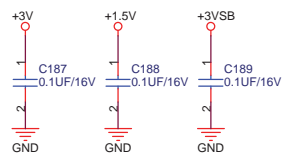
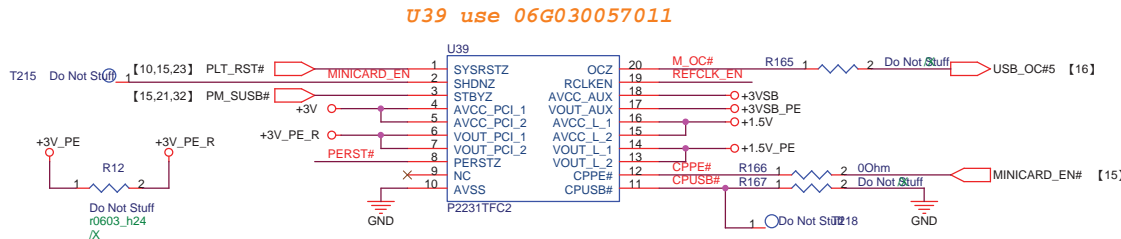
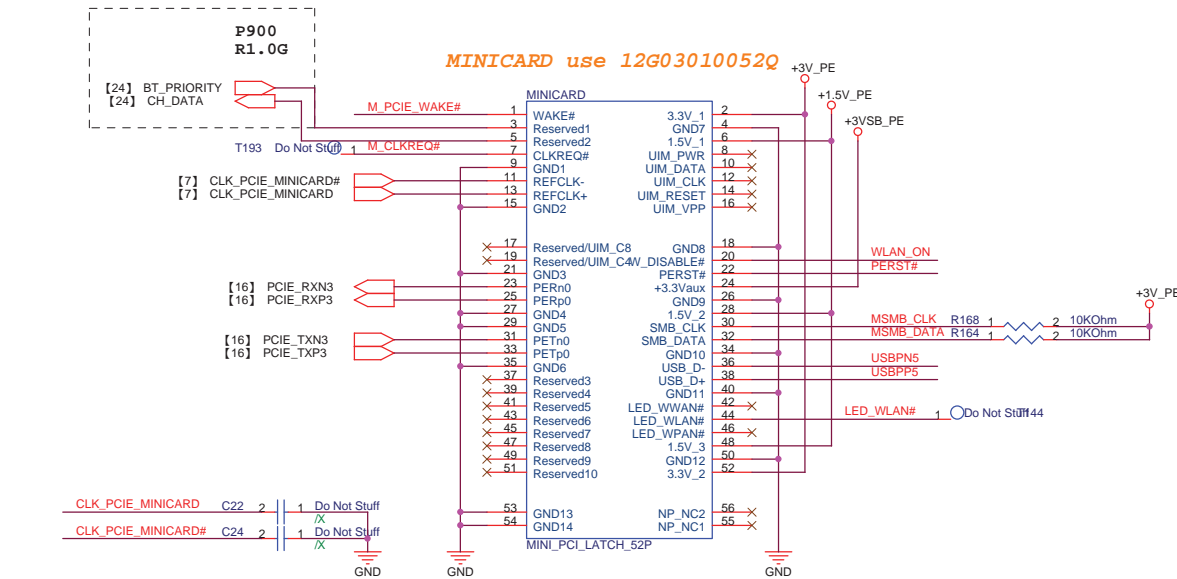
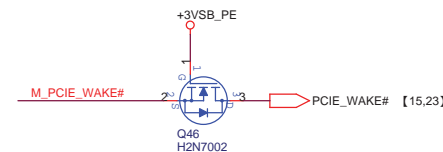
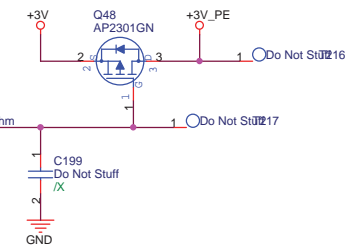
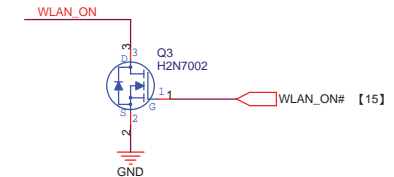
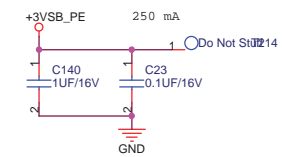
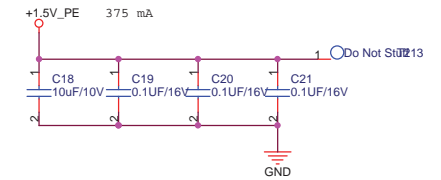


P900\_R1.1G\_WO\_FLASH

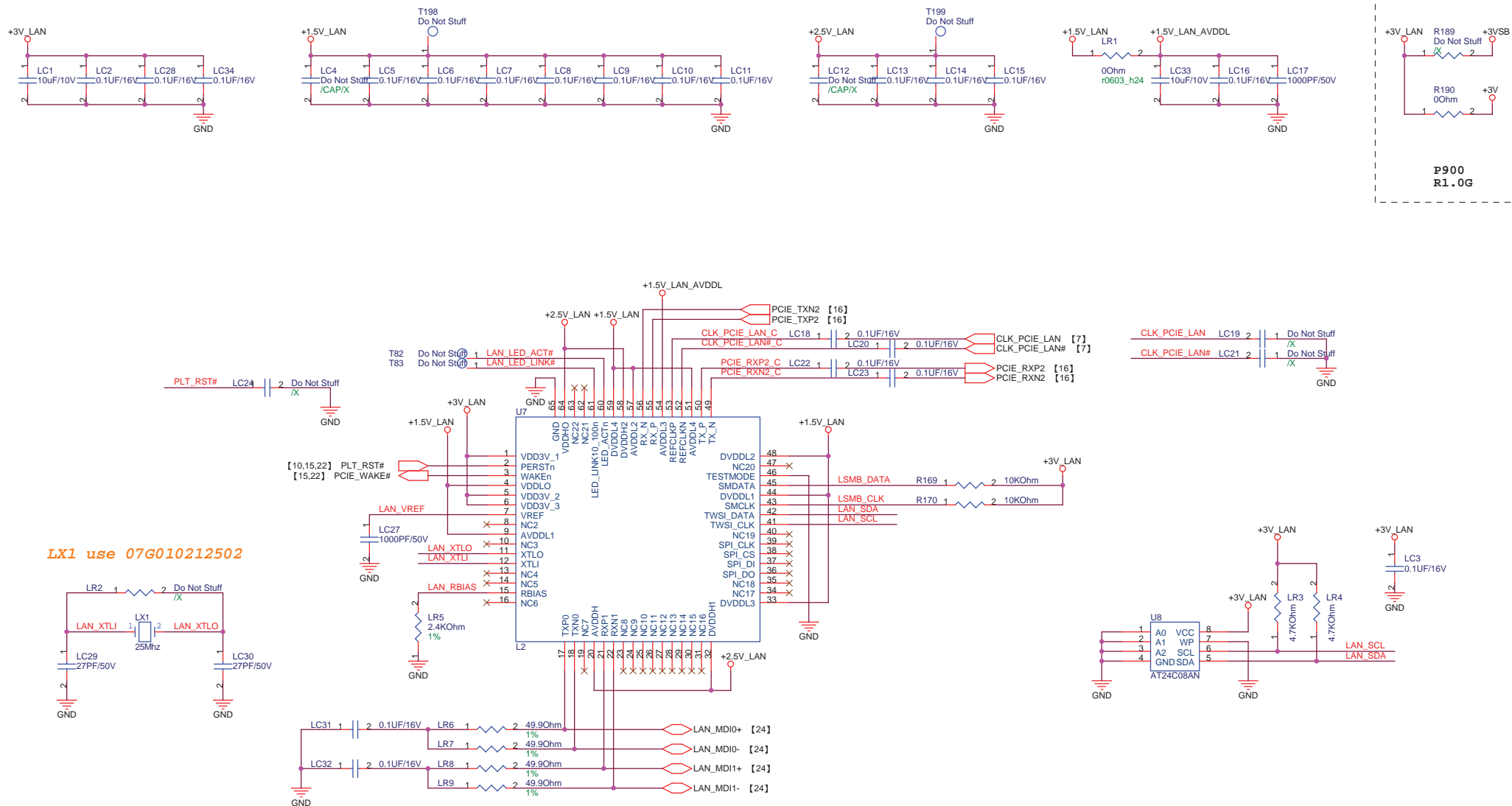
ASUS		Title : LCD Conn	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	21 of 47

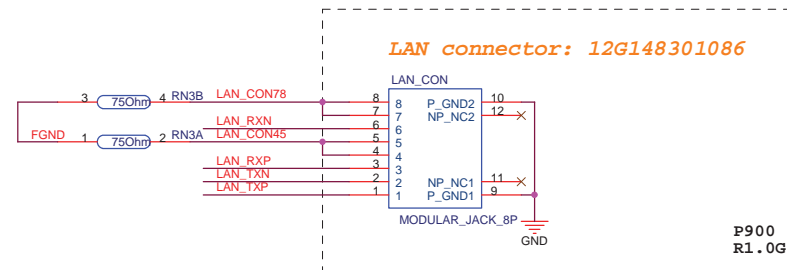
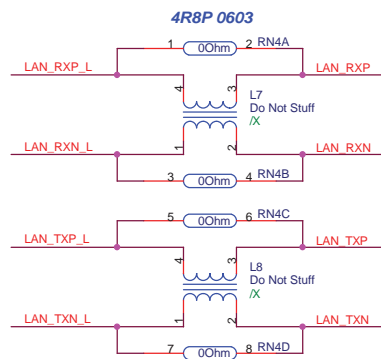
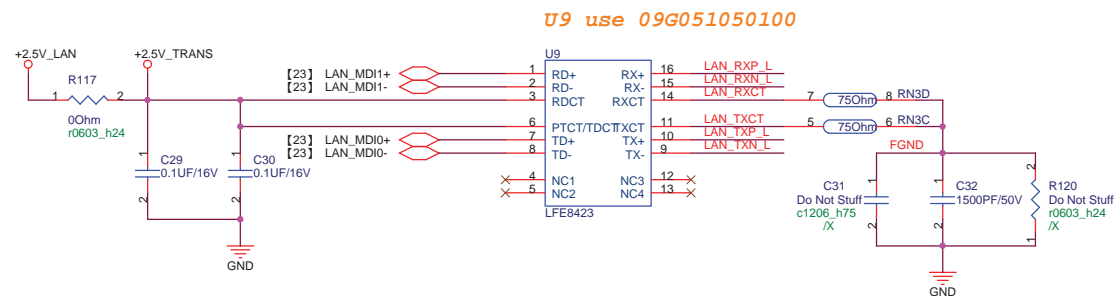
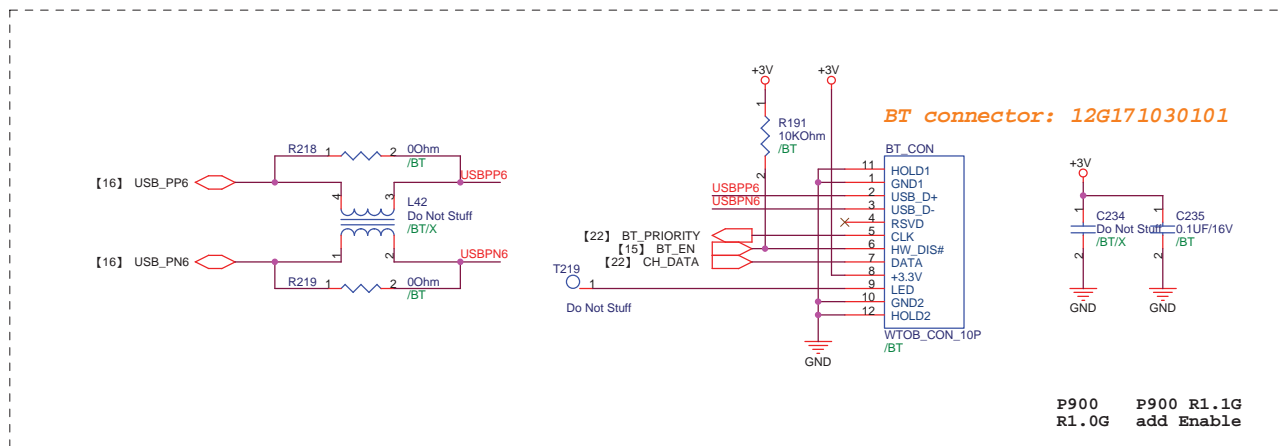


MINI CARD NUT(1.6mm) \*2



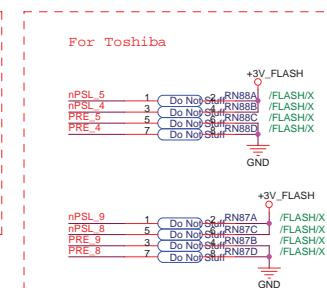
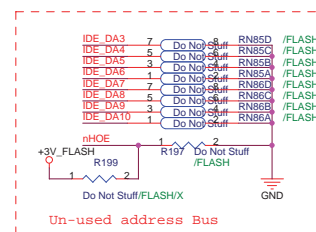
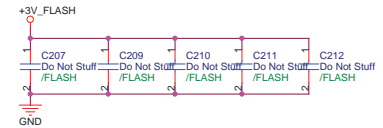






P900\_R1.1G\_WO\_FLASH

<b>ASUS</b>		Title : RJ45/BlueTooth	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008		Sheet	24 of 47



**H: Slave**  
**L: Master**

+3V\_FLASH

R196 Do Not Stiff SLASH/X

R198 Do Not SLASH/X

R200 Do Not SLASH

R201 Do Not SLASH

R202 Do Not SLASH/X

R204 Do Not SLASH/X

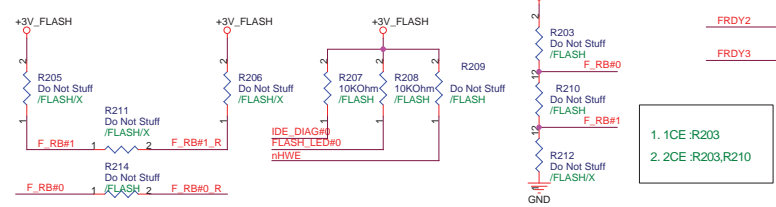
CSEL#

GPIO0

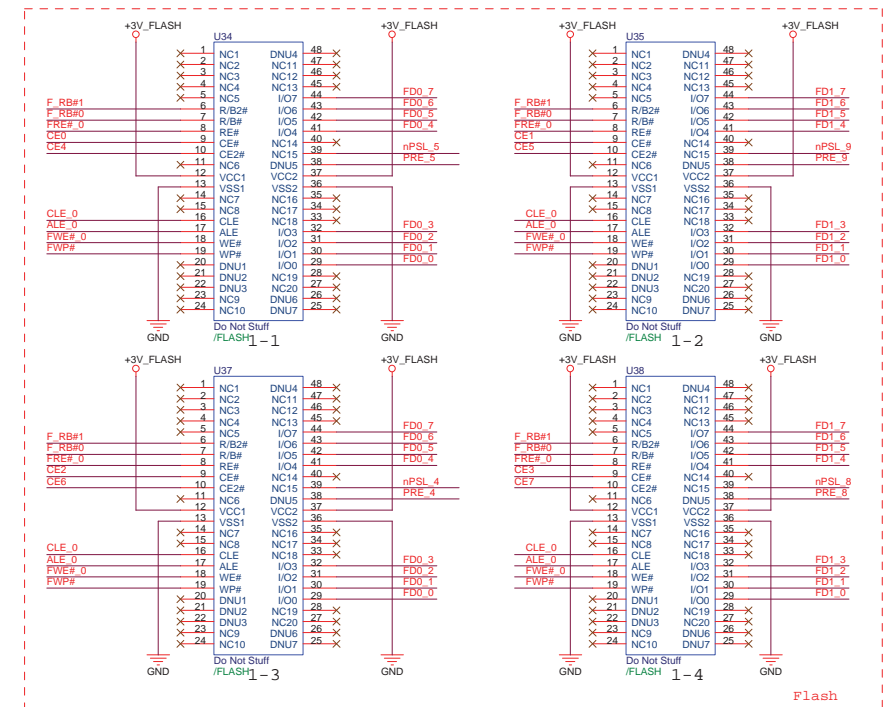
GPIO2

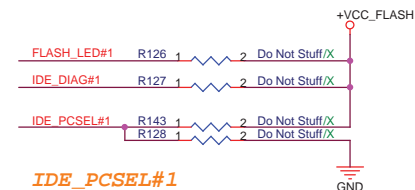
FRDY2

FRDY3

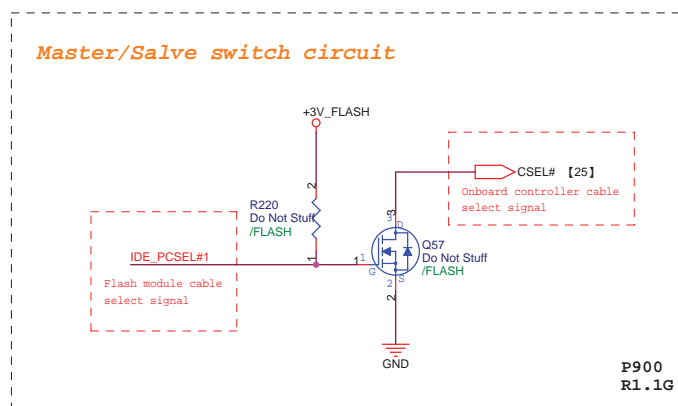
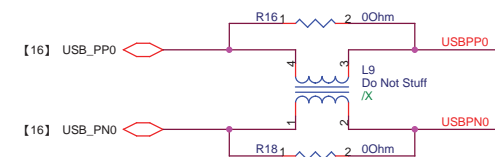
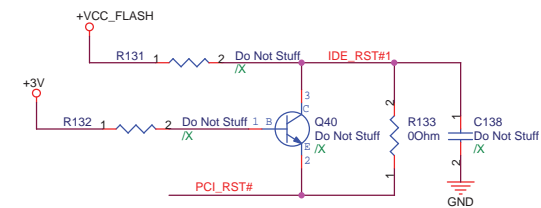
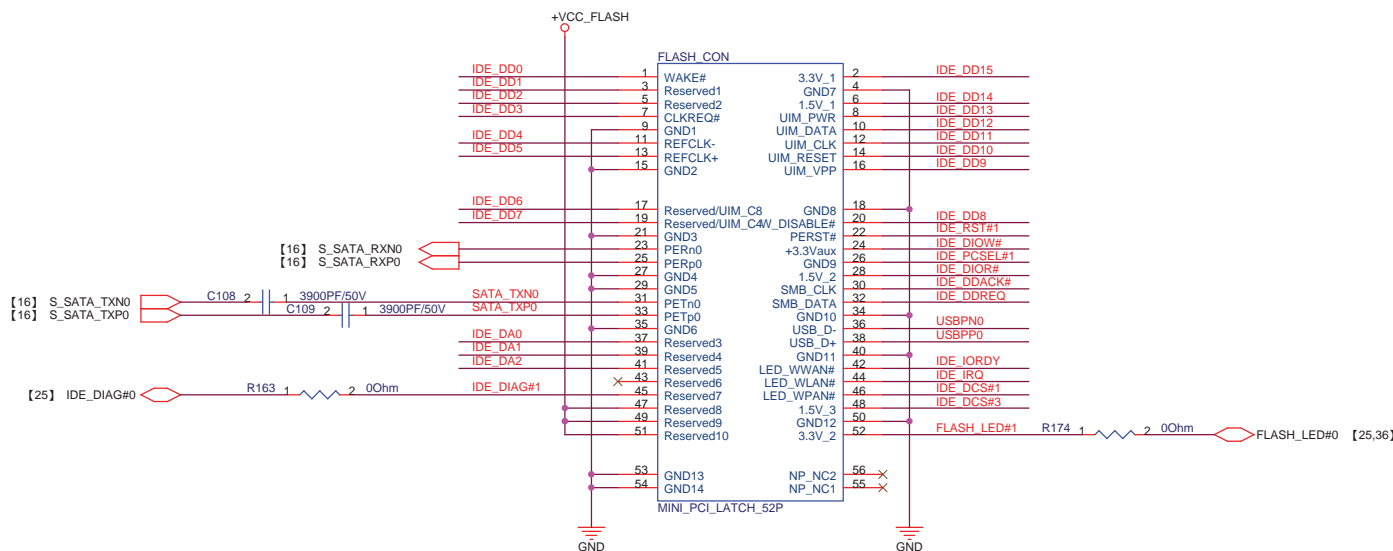
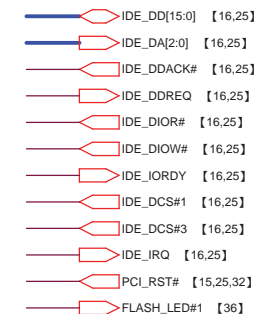


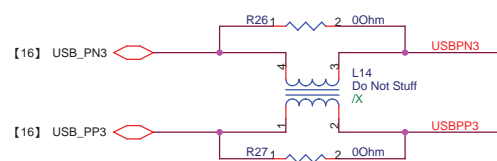
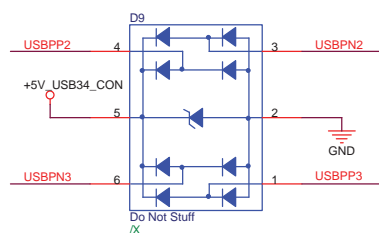
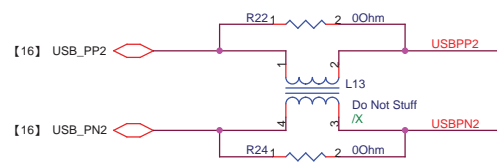
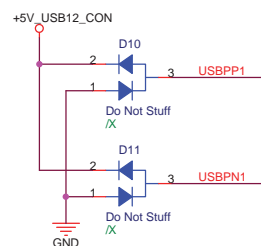
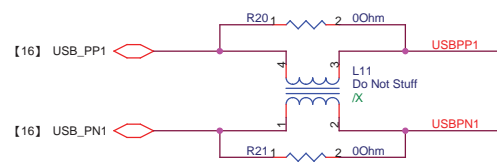
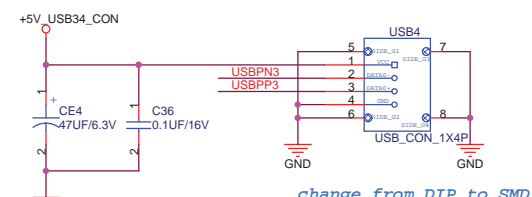
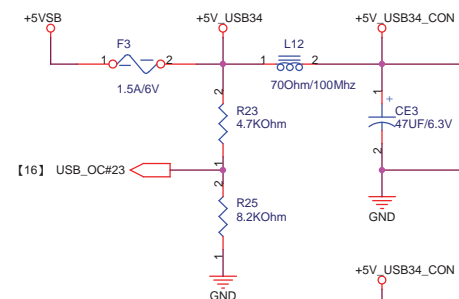
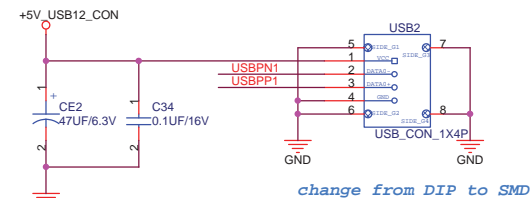
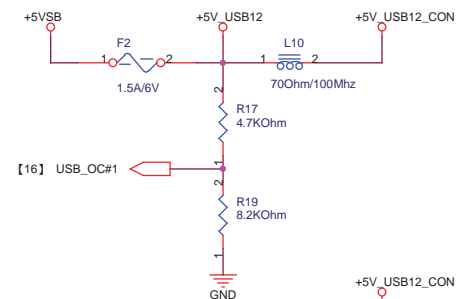
1. 1CE :R203
2. 2CE :R203,R210

[illegible][illegible]



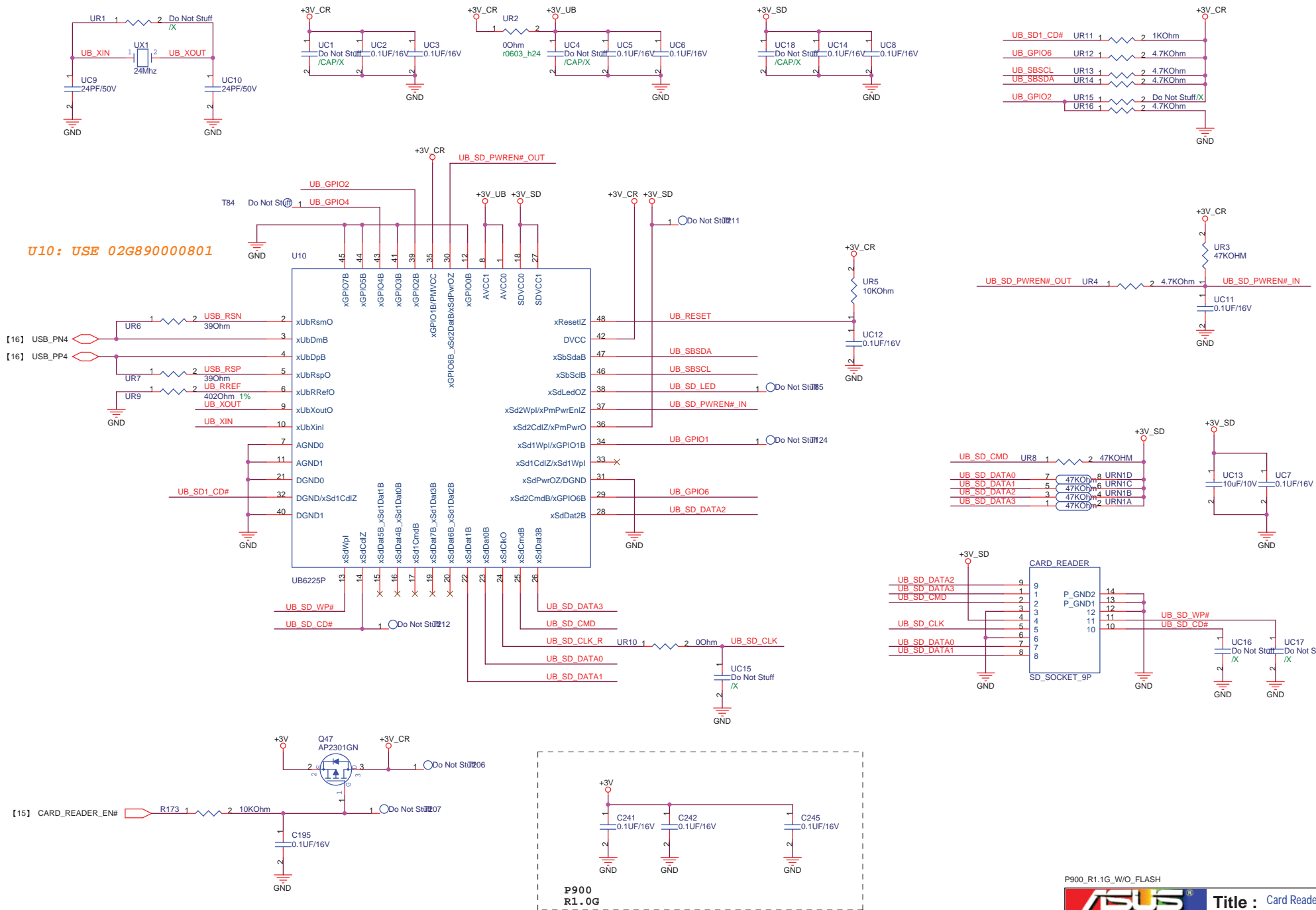
```
IDE_PCSEL#1
H: Slave
L: Master
```

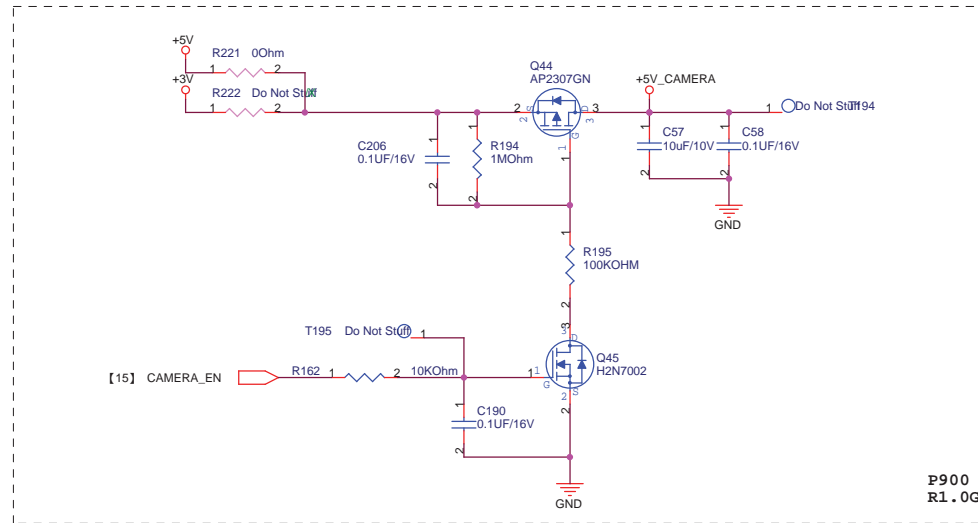
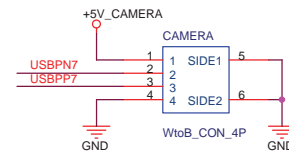
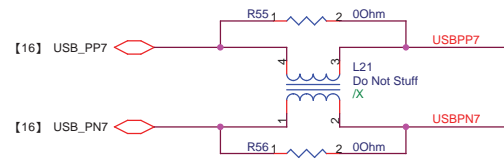




P900\_R1.1G\_WO\_FLASH

<b>ASUS</b>		Title : USB Port	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008		Sheet	27 of 47





P900  
R1.0G

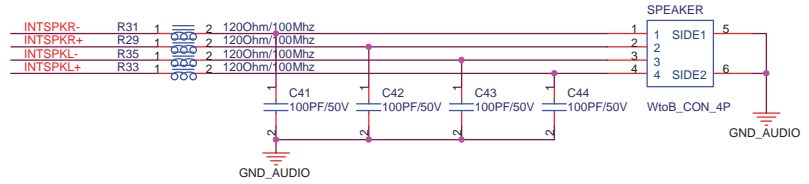
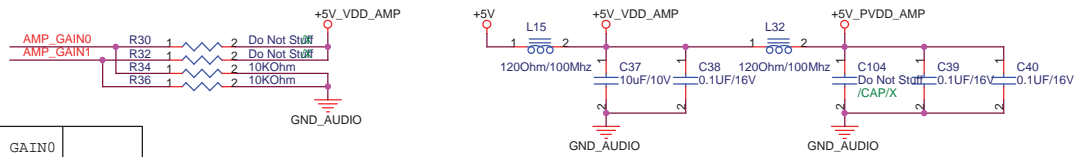
P900\_R1.1G\_WO\_FLASH

<b>ASUS</b>		<b>Title : Camera Conn</b>	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size A3	Project Name <b>P900</b>	Rev 1.2G	
Date: Wednesday, February 27, 2008		Sheet 29 of 47	

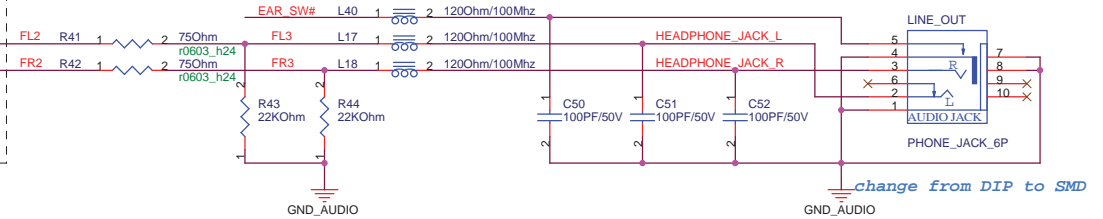
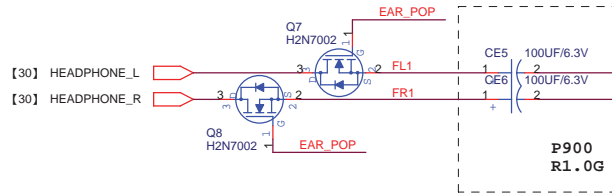
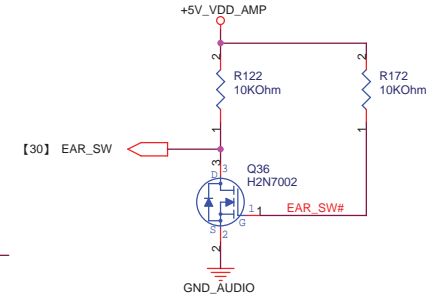
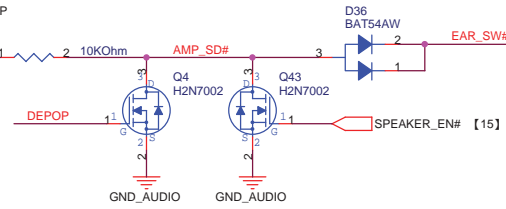
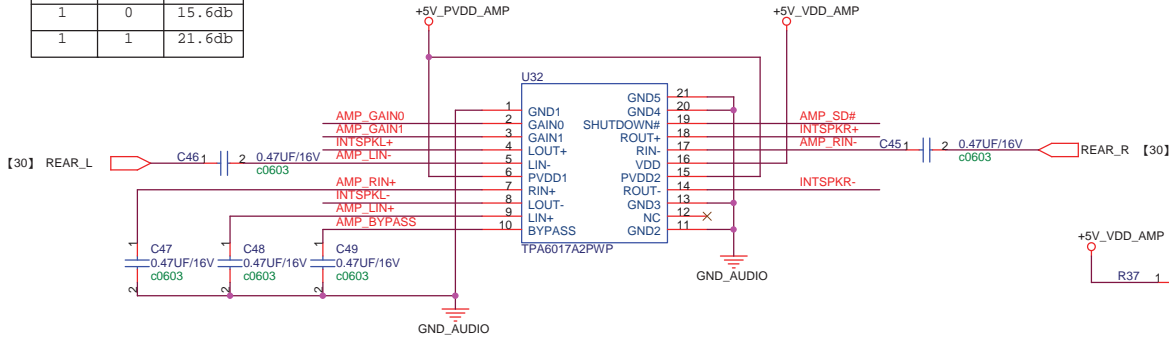




GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



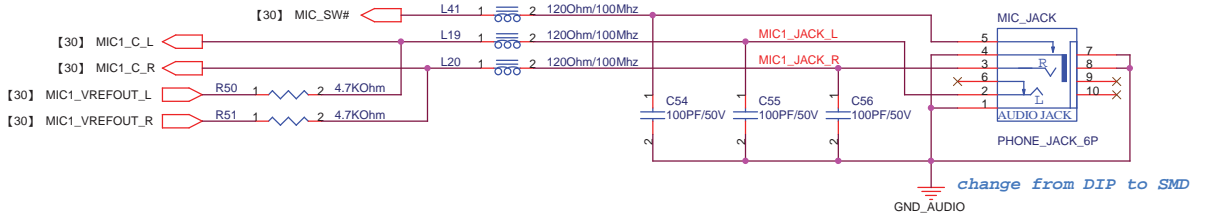
**R29, R31, R33, R35 use Bead 09G013120114 for EMI**



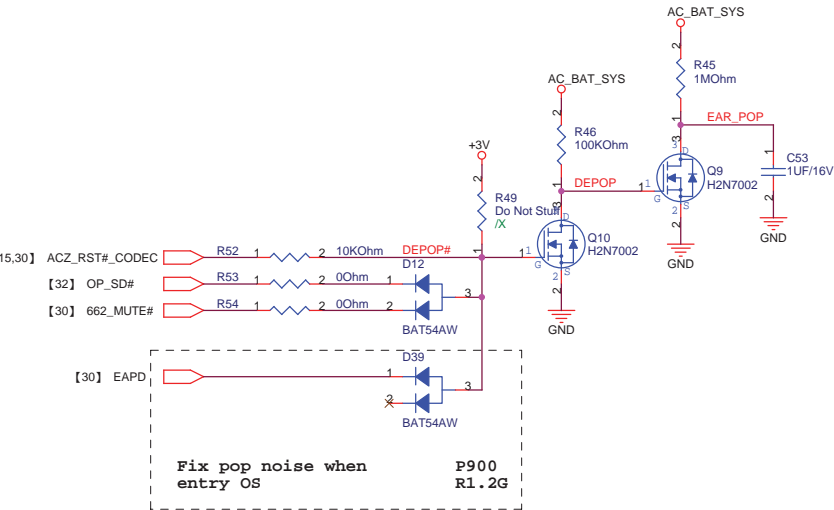
**LINE\_OUT use 12G14040106N**

**change from DIP to SMD**

**MIC\_JACK use 12G14040106G**



**change from DIP to SMD**



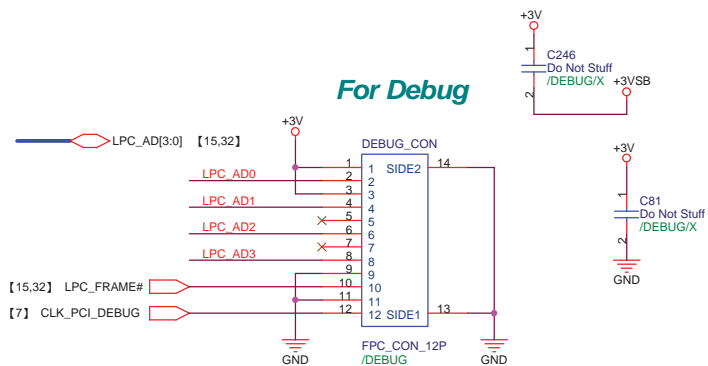
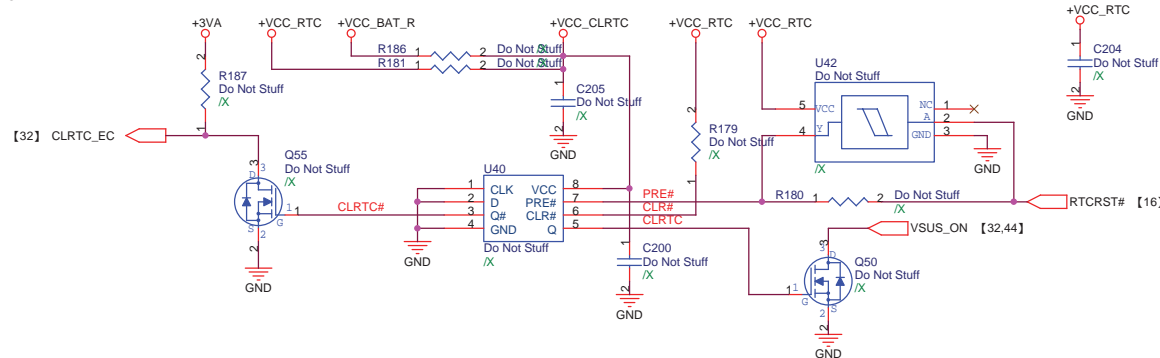
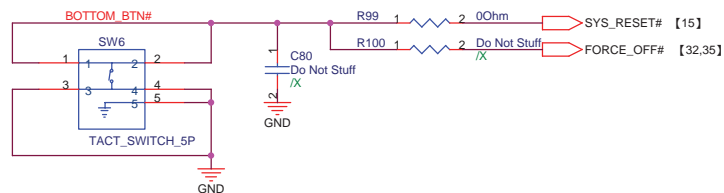
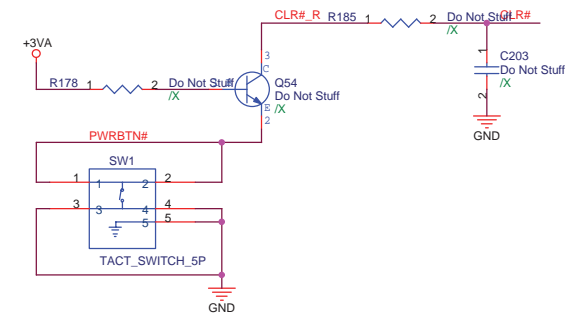
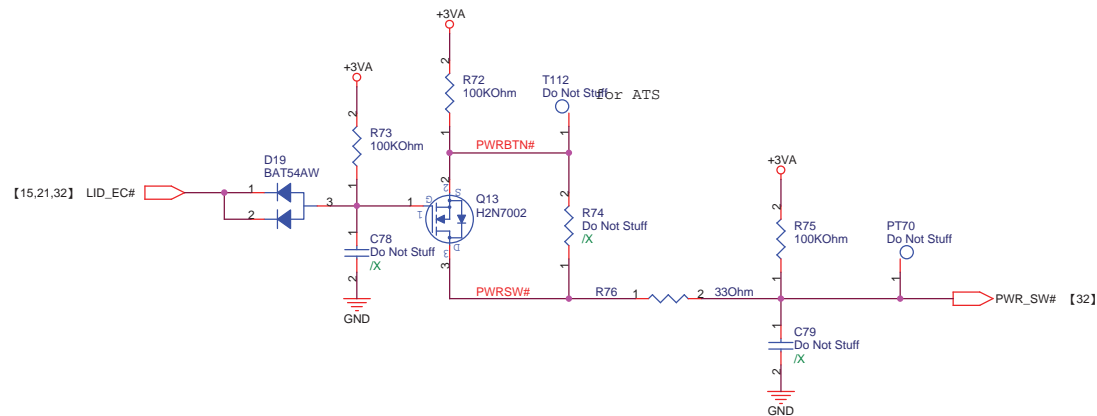
**Fix pop noise when entry OS**

**P900 R1.2G**

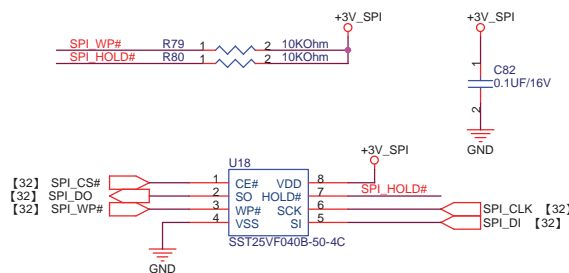
P900\_R1.1G\_WO\_FLASH

<b>ASUS</b>		<b>Title : Audio_AMP_Jack</b>	
ASUSTek Computer INC.		Engineer: <b>Tiansen_Wu</b>	
Size	Project Name	Rev	
A3	<b>P900</b>	1.2G	
Date: Wednesday, February 27, 2008		Sheet	31 of 47

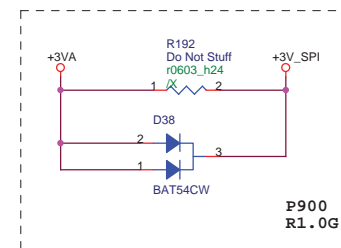




Debug Card cable use Z96 Touch Pad cable, P/N:  
14G124110126, 14G124110120, 14G124110121  
14G124110124, 14G124110125



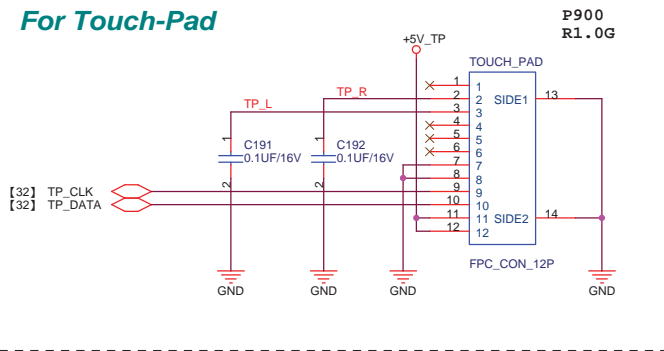
U18 use 05G001002900 & 05G00100F130



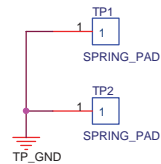
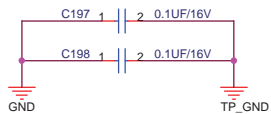
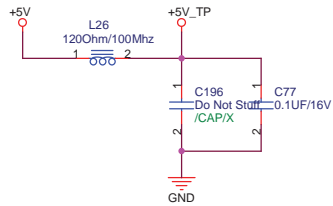
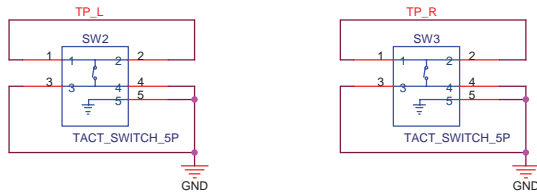
P900\_R1.1G\_WO\_FLASH

ASUS		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008		Sheet	33 of 47

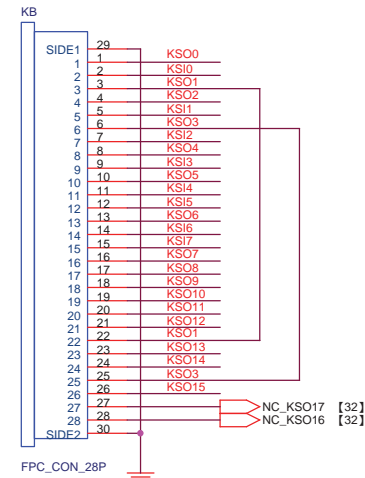
## For Touch-Pad



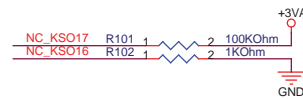
SW2, SW3 use 12G09103305N



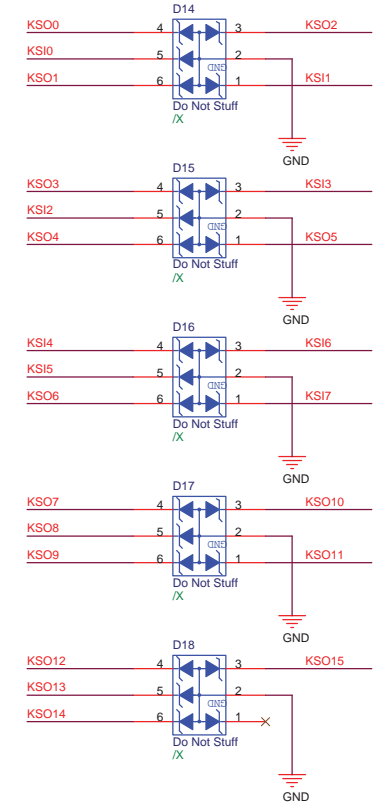
## For Keyboard



KSO15 1 Do Not Stuff 88  
KSI0 1 Do Not Stuff 89  
KSO3 1 Do Not Stuff 90

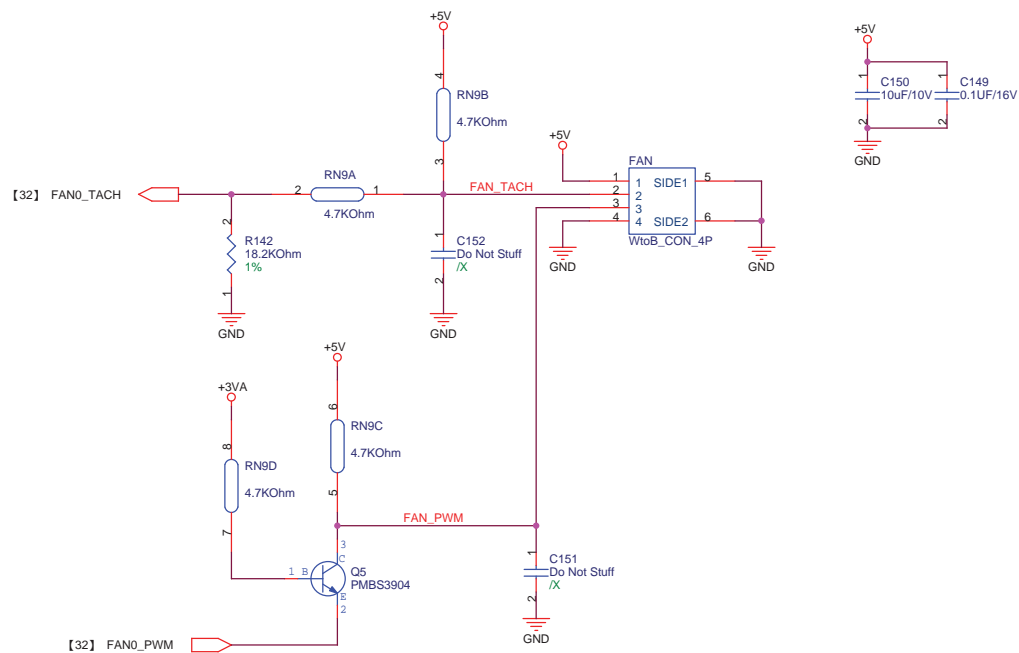
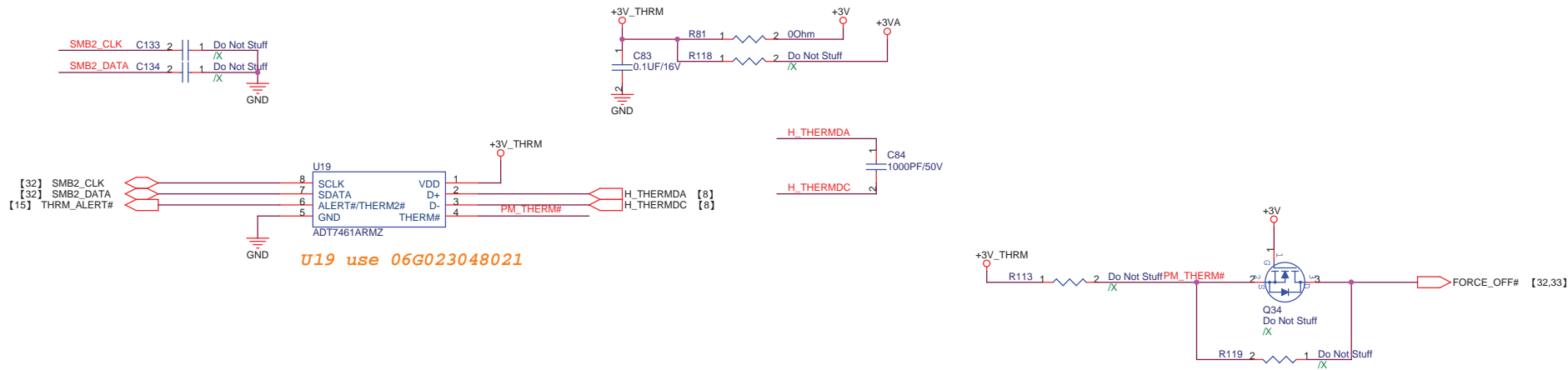


KSO[15:0] [32]  
KSI[7:0] [32]



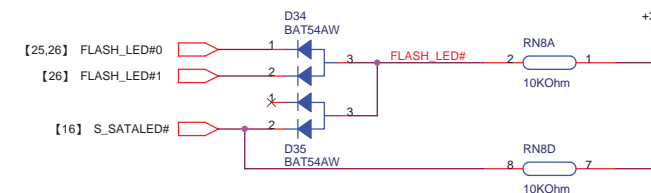
P900\_R1.1G\_WO\_FLASH

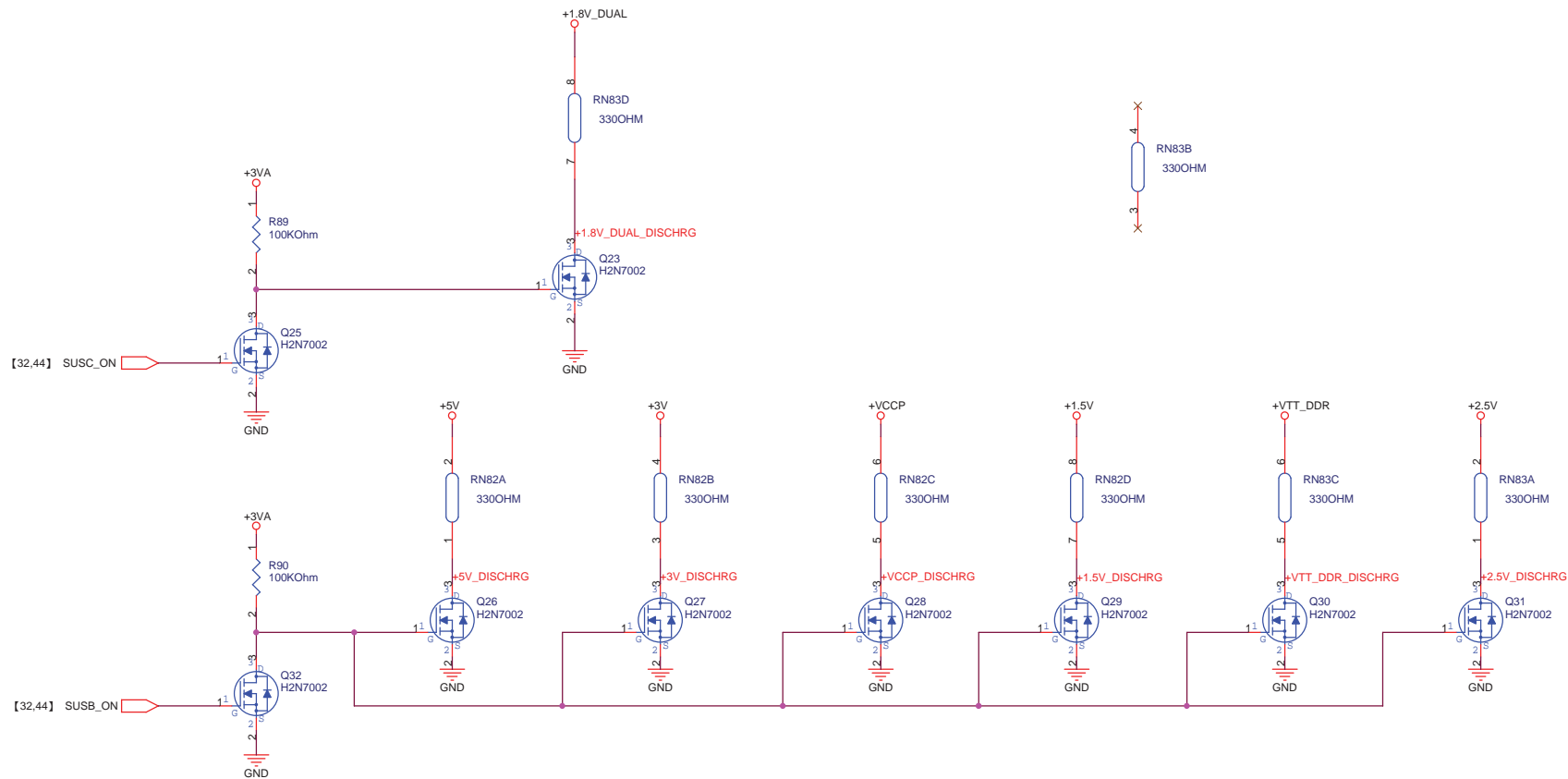
<b>ASUS</b>		Title : KB_Touch Pad	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	34 of 47



P900\_R1.1G\_WO\_FLASH

<b>ASUS</b>		<b>Title : Thermal Sensor_FAN</b>	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name	Rev	
A3	<b>P900</b>		1.2G
Date: Wednesday, February 27, 2008		Sheet	35 of 47



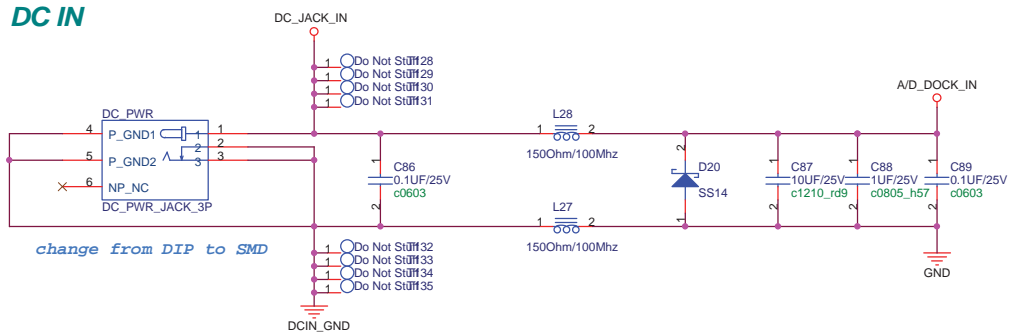


P900\_R1.1G\_WO\_FLASH

<b>ASUS</b>		<b>Title : Discharge</b>	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name		Rev
A3	<b>P900</b>		1.2G
Date: Wednesday, February 27, 2008		Sheet	37 of 47

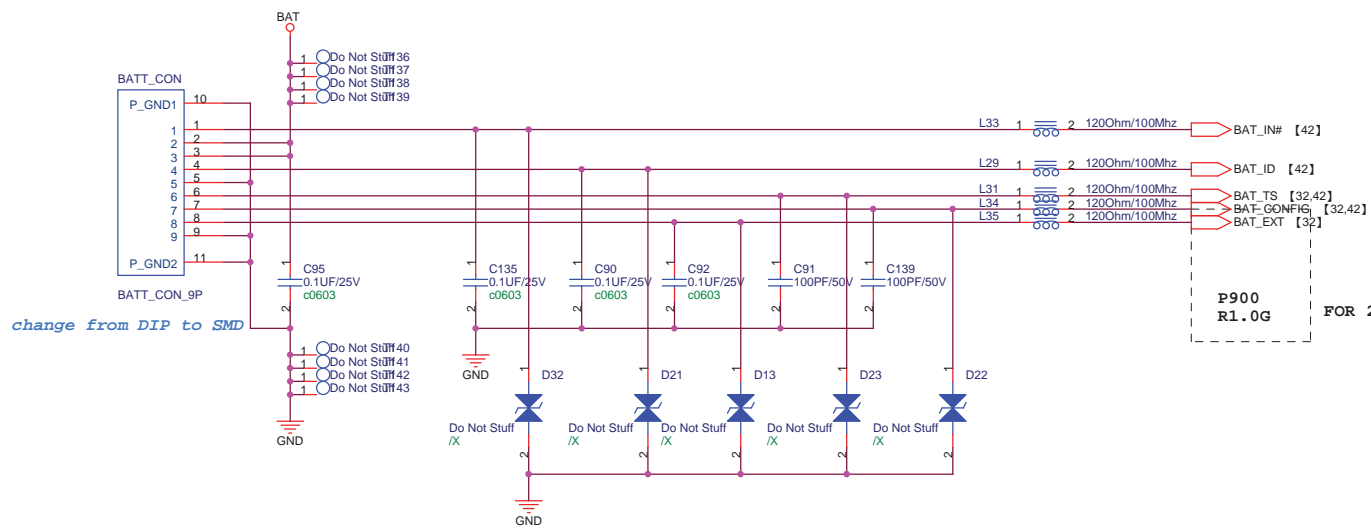


## DC IN



change from DIP to SMD

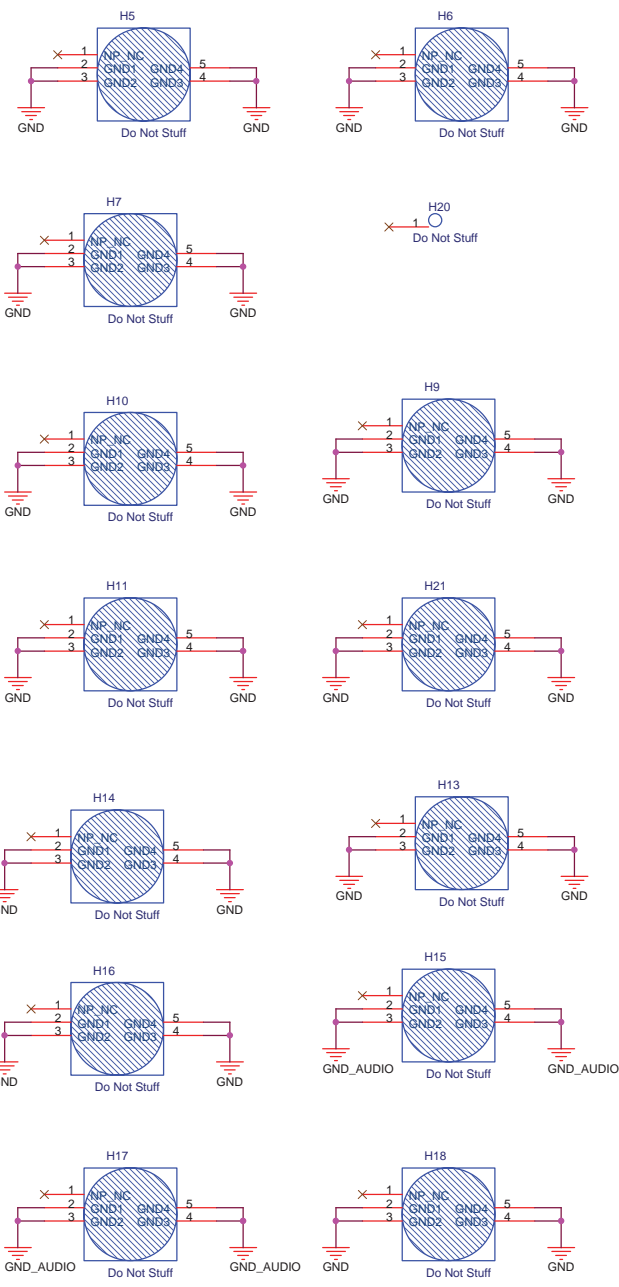
## BAT IN

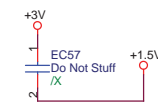
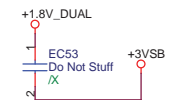
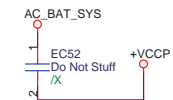
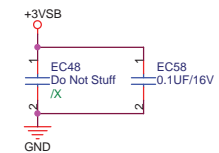
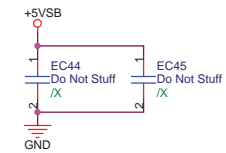
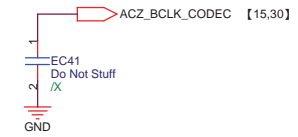
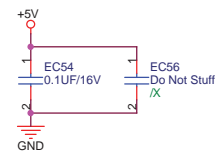
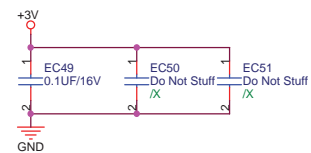
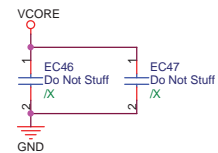
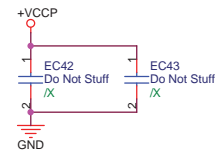
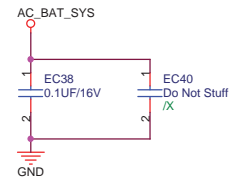
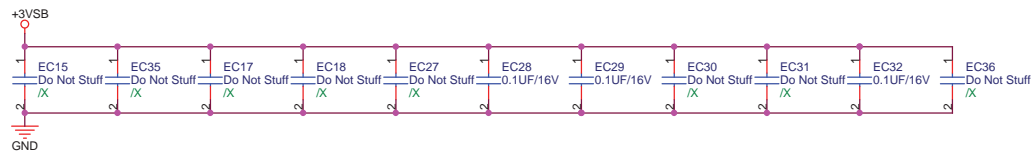
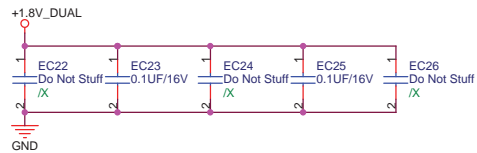
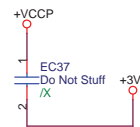
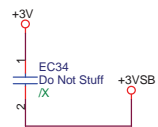
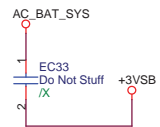
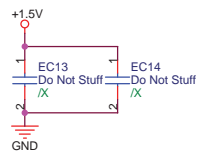
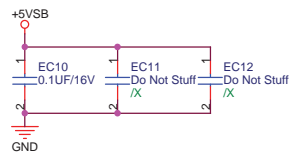
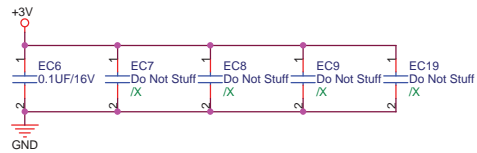
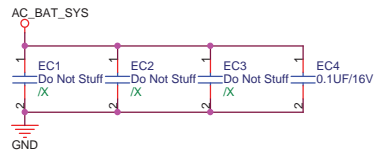


change from DIP to SMD

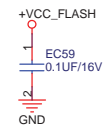
P900  
R1.0G  
FOR 2.9Ah battery

P900_R1.1G_WO_FLASH		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	38 of 47



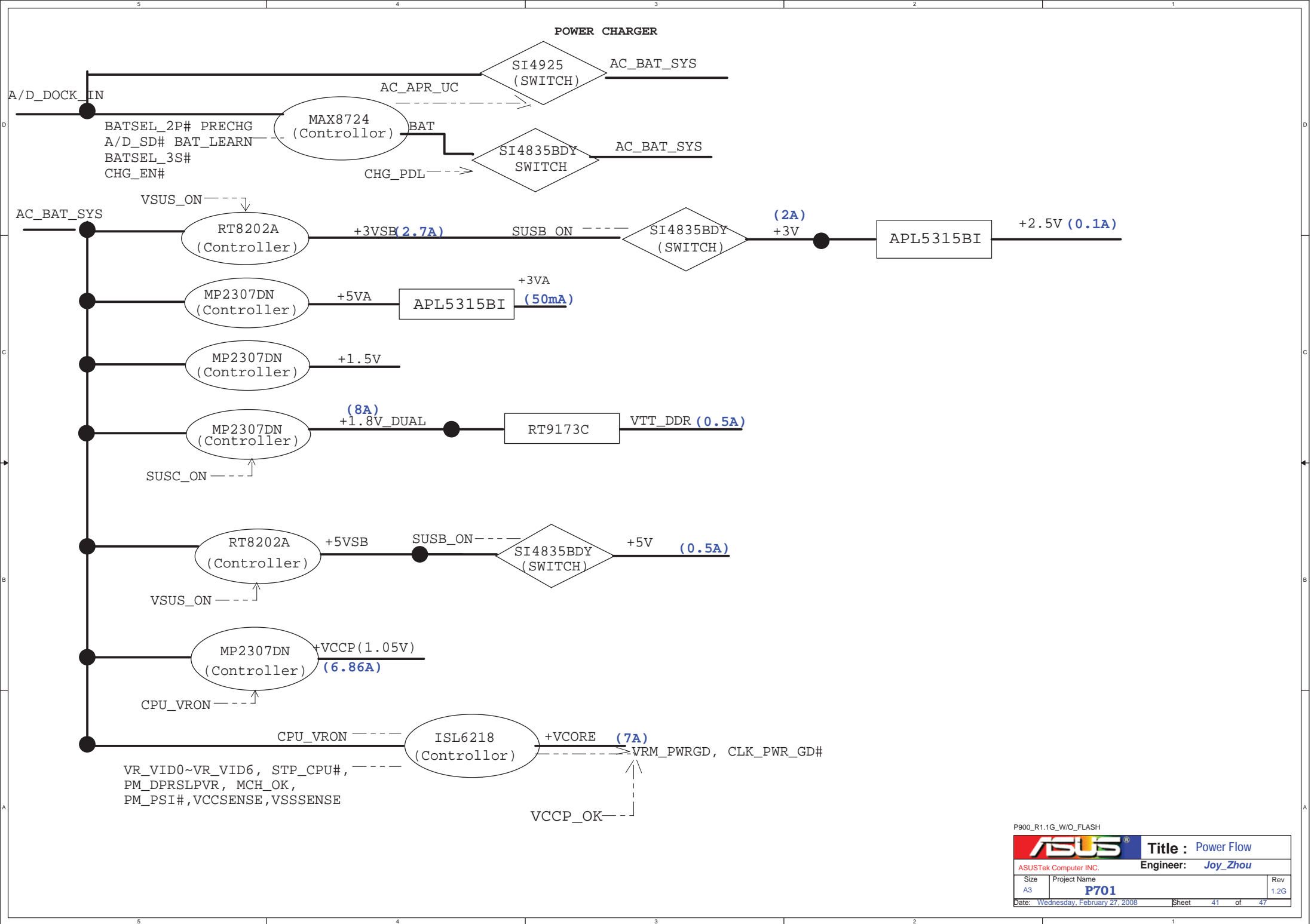


P900  
R1.00



P900\_R1.1G\_WO\_FLASH

<b>ASUS</b>		Title : EMI	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	40 of 47



**Prevent Input from 19V :**  
Adaptor > 14.1V, PQ1 & PQ11 Turn-off  
Adaptor < 14.1V, PQ1 & PQ11 Turn-on

**Fast Charging :**  
Adaptor > 11V, PQ4 Turn-on, Adaptor current~2.85A  
Adaptor < 11V, PQ4 Turn-off, Adaptor current~2.17A

VREFIN = 3.396V  
MAX8724\_REF : 4.096V  
MAX8724\_LDO : 5.4V

**Pre-Charging Mode :**  
Precharging current = 150mA  
Vctcl = 169.8mV

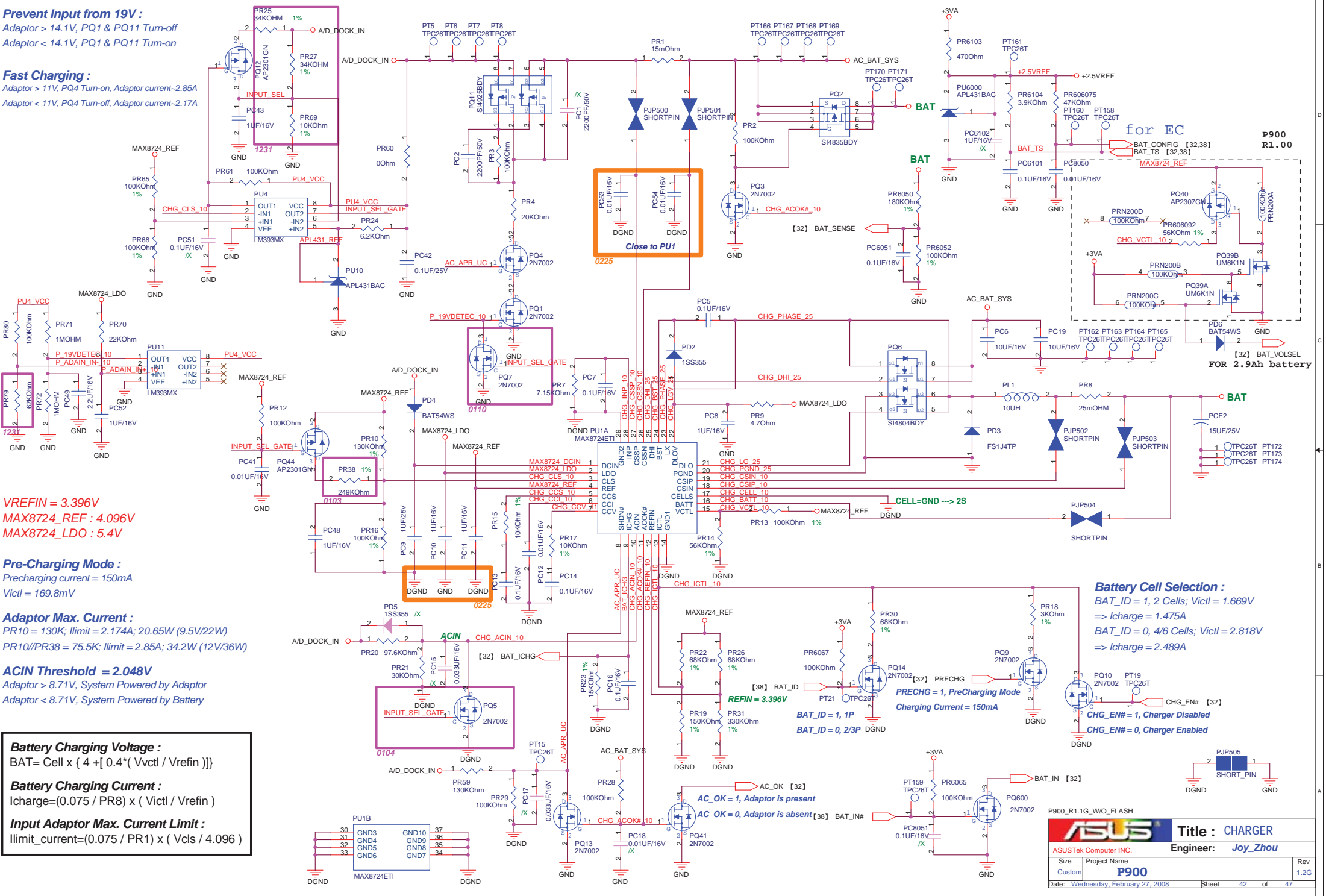
**Adaptor Max. Current :**  
PR10 = 130K; Ilimit = 2.174A; 20.65W (9.5V/22W)  
PR10//PR38 = 75.5K; Ilimit = 2.85A; 34.2W (12V/36W)

**ACIN Threshold = 2.048V**  
Adaptor > 8.71V, System Powered by Adaptor  
Adaptor < 8.71V, System Powered by Battery

**Battery Charging Voltage :**  
 $BAT = Cell \times \{ 4 + [ 0.4 * ( V_{ctcl} / V_{refin} ) ] \}$

**Battery Charging Current :**  
 $I_{charge} = (0.075 / PR8) \times ( V_{ctcl} / V_{refin} )$

**Input Adaptor Max. Current Limit :**  
 $I_{limit\_current} = (0.075 / PR1) \times ( V_{cls} / 4.096 )$



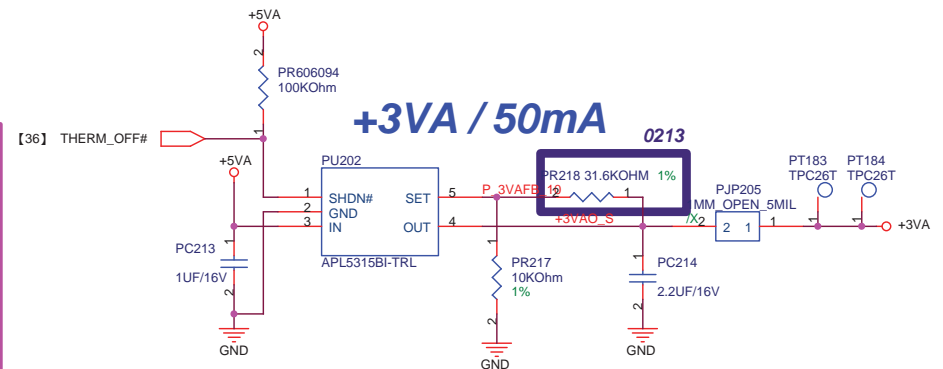
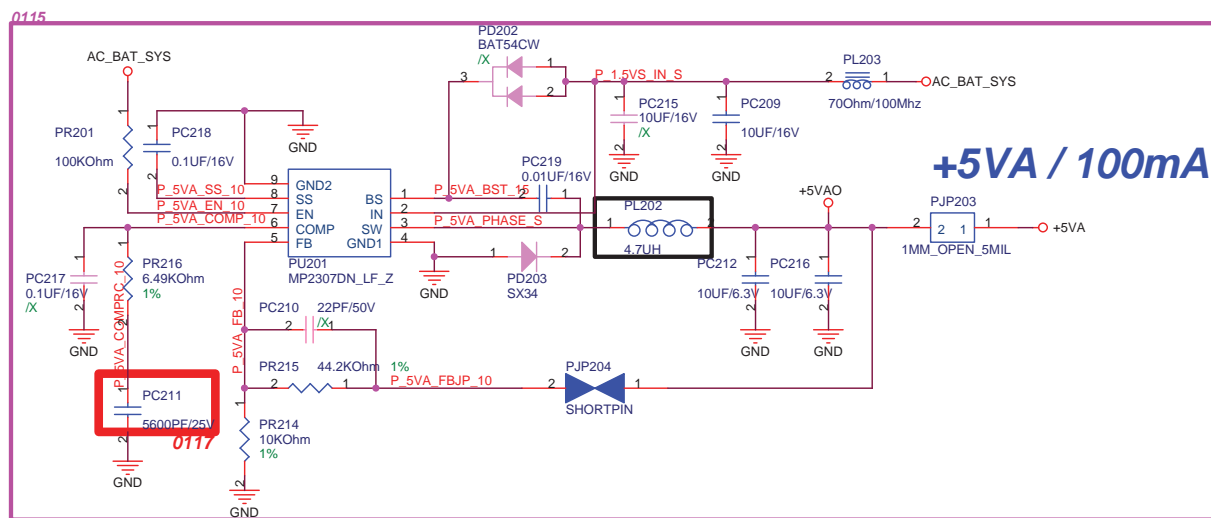
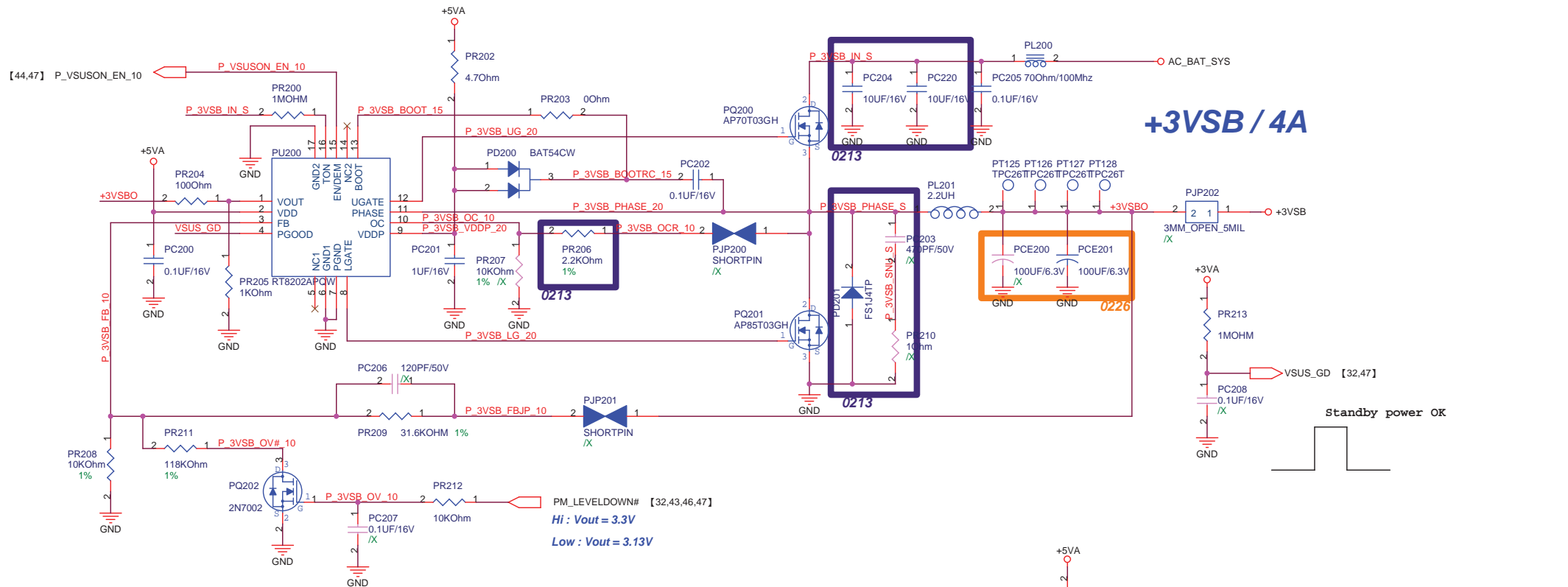
**Battery Cell Selection :**  
BAT\_ID = 1, 2 Cells; Vctcl = 1.669V  
=> Icharge = 1.475A  
BAT\_ID = 0, 4/6 Cells; Vctcl = 2.818V  
=> Icharge = 2.489A

PRECHG = 1, PreCharging Mode  
Charging Current = 150mA

CHG\_EN# = 1, Charger Disabled  
CHG\_EN# = 0, Charger Enabled



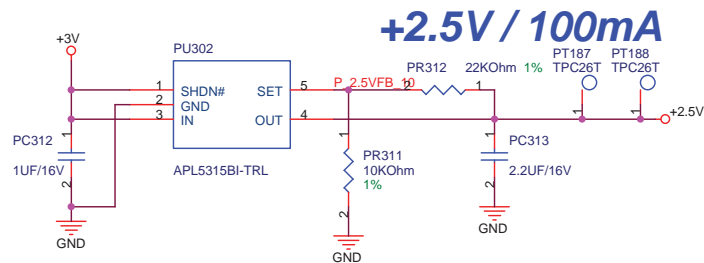
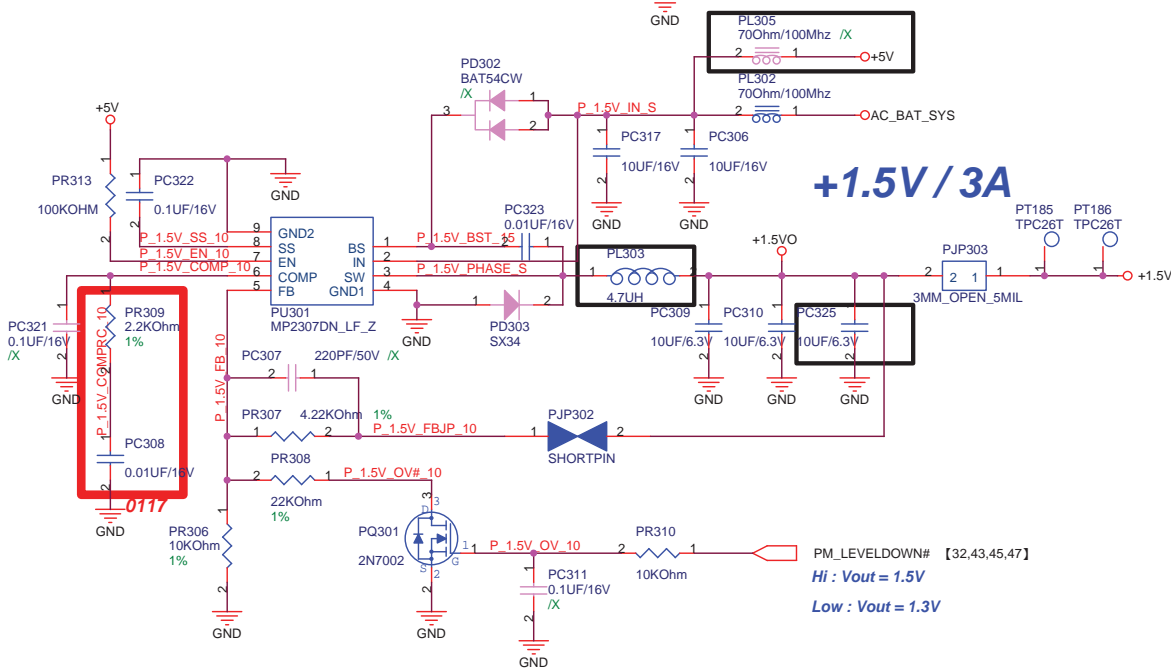
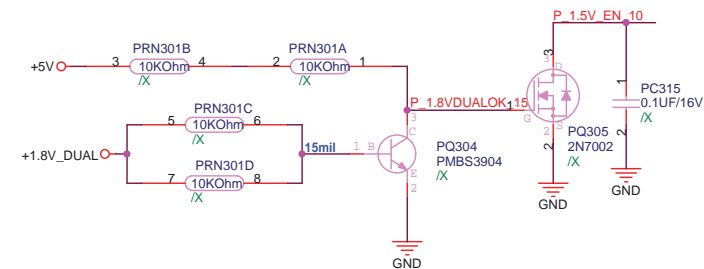
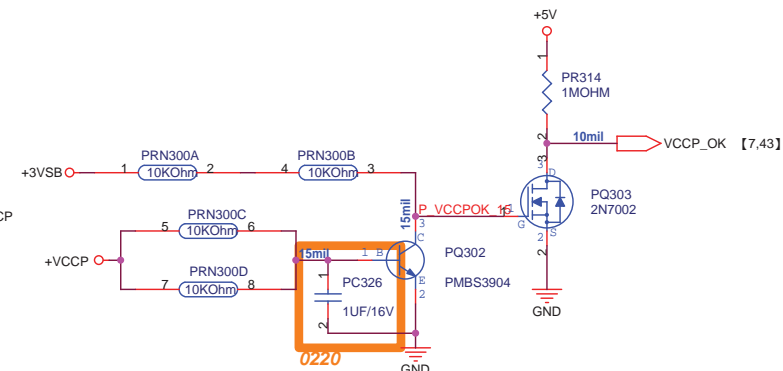
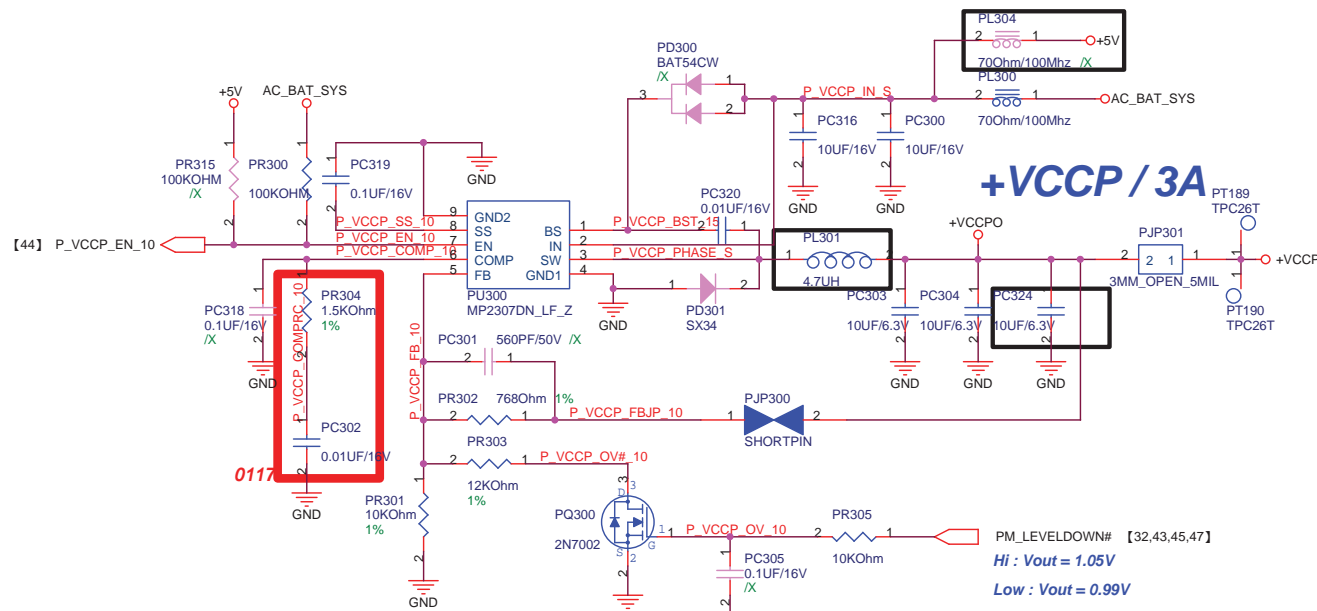




P900\_R1.1G\_W/O\_FLASH

<b>ASUS</b>		Title : 3VA_3VSB	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size B	Project Name <b>P900</b>	Rev 1.2G	
Date: Wednesday, February 27, 2008		Sheet 45	of 47





P900\_R1.1G\_W/O\_FLASH

<b>ASUS</b>		Title : 1.05V_1.5V_2.5V	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	Rev	
B	P900	1.2G	
Date: Wednesday, February 27, 2008	Sheet	46	of 47

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